SOLID STATE ELECTRONICS LABORATORY

JSEP ANNUAL REPORT

1 July, 1989 through 30 June, 1990

James S. Harris, Jr.
JSEP Principal Investigator
and Program Director

(415) 723-9775

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Joint Services Electronics Program
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Abstract

This is the annual report of the research conducted at the Stanford Electronics Laboratories under the sponsorship of the Joint Services Electronics Program from 1 July 1989 through 30 June 1990. This report summarizes the area of research, identifies the most significant results and lists the dissertations and publications sponsored by the contract DAAL03-88-C-0011.

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JSEP ANNUAL REPORT

July 1, 1989 - January 10, 1991

Introduction

The JSEP contract supports a program of unclassified basic research in electronics conducted by faculty members of the Electrical Engineering Department of Stanford University as a component of the research program of the Stanford Electronics Laboratories. The Stanford Electronics Lab JSEP Director and Principal Investigator is Professor James Harris. He is responsible for the selection of the best individual proposals, coordination between Stanford and the JSEP TCC and coordination between the selected areas of the JSEP Program. In planning the JSEP Program at SEL, a general objective is to develop new projects with 3-4 years of JSEP sponsorship, leading to a transition to more conventional DoD or other agency program funding. Since this type of funding often requires 12-18 months in the proposal, evaluation and budgeting stages, the flexibility in JSEP funding allows us to seize new opportunities and initiate programs which might otherwise be delayed for a significant period.

This report covers an eighteen month period because our overall funding period was reduced to 30 months to synchronize the SEL JSEP program with the Ginzton Lab JSEP cycle and also to fit better into the DoD budget cycle.

Two projects substantially changed course during this period: Unit 3, under Professor Plummer and Unit 4, under Professor Saraswat. Both are aimed at application of heterojunctions and new device and materials concepts as a result of rapid progress in the SiGe alloy system and its potential integration with more conventional Si IC technology. These thrusts are being carried forward into the new JSEP program. Highlights of three projects are described below. Following these highlights, the specific objectives and progress in each work unit are reported.

Low temperature processing is becoming increasingly important. Si films become amorphous when deposited below 600°C, thus limiting the quality of low temperature films for thin film transistors (TFT) and poly gates for MOSFETs. Poly SiGe films have been deposited by LPCVD at 500°C with 0.2 the sheet resistance for poly Si films and 0.5 the sheet resistance for poly Si films deposited at 900°C. The SiGe films may produce vastly improved TFTs on glass for large area displays as well as lower resistivity poly gates and adjustment of the gate workfunction in conventional VLSI technology.

The Molecular Beam Epitaxial (MBE) growth of high temperature superconductors is a strong collaboration with researchers at Varian Associates and has resulted in a substantial DARPA contract. The ability of MBE to grow in-situ layered, metastable-like compounds has been demonstrated. This is a major step in the development of artificially layered combinations of perovskite-related compounds. Low temperature growth is required to grow metastable layered $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ structures, particularly for any attempt to combine these compounds with other electronic materials. A We have demonstrated the first true single crystal growth of $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ by any technique. This was achieved by in-situ MBE growth on a vicinal or misoriented $SrTiO_3$ substrate.

One of the basic assumptions in neural networks is that we allow the neural elements to take on an unbounded number of inputs, i.e., we allow unbounded fan-in. By exploiting this feature, we have to shown the following interesting results: the sum and product of two n-bit numbers, and sorting of n n-bit numbers can all be done with 4 unit delays with neural networks. We have extended our results to more complicated functions and have shown that exponentiation and division can be computed with 5 unit delays, and multiple product can be computed with 6 unit delays, with neural networks.

The technical knowledge developed under the JSEP contract is widely disseminated through sponsor reviews, presentations of papers at technical meetings, publications in the open literature, discussions with visitors to the laboratories, and publication of laboratory technical reports.

Unit: 1

TITLE: Molecular Beam Epitaxy of High T_c Superconductors and Investigation of Quantum Well Structures

Principal Investigator: James S. Harris, Jr.

Graduate Students: Darrell G. Schlom and Peng Cheng

A. MOLECULAR BEAM EPITAXY OF HIGH T_c SUPERCONDUCTORS

1. Scientific Objectives:

The discovery of a new class of materials which exhibit superconductivity at unprecedented temperatures has opened new possibilities for future electronic devices. The polycrystalline nature of the ceramic forms of these materials is likely to be unsuitable for electronics applications. In addition, the very short coherence lengths of these superconductors has made it difficult to prepare thin film tunnel junctions in the usual ways. The ideal form of these materials is thus likely to be that of epitaxial films, prepared in such a way that composition and structure can be controlled at the atomic layer level. Because of the controlled layering possible with molecular beam epitaxy (MBE), we have focused on syntactic intergrowth of $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ phases where n ranges from 1 to 5. We have chosen this family of superconductors because the free energy of formation appears virtually degenerate for all phases of these materials, thus bulk and even controlled thin film growth results in small polycrystalline regions of different phases. Not only single phase material, but true single crystal material would be desirable for device fabrication. Further, controlled layering offers an unparalleled opportunity to fabricate metastable superlattice mixtures to test high T_c theories, and may allow the growth of higher temperature superconducting compounds, once a proper theory is established. It is with these goals in mind that we have undertaken a systematic study of the growth of $Bi_2Sr_2Ca_{n-1}Cu_nO_{2n+4}$ by MBE.

2. Summary of Research:

The work described here is the product of a collaboration between the MBE groups at Stanford University and the Varian Research Center and the High T_c Thin Film group at Stanford. This work was initially supported by JSEP, Varian and NSF, respectively, for each of the above groups. The ability to support this project immediately produced significant results and led to DARPA support of a joint Varian/Stanford MBE contract. Since this DARPA program now supports a majority of the MBE work, only a summary of

the highlights of the project are described

The growth of fully oxidized compounds by MBE offers significant challenges compared to its conventional use in the growth of semiconductor compounds. Clearly, in order to realize layered metastable structures, a low temperature, in-situ growth method is required. Further an activated species of oxygen is necessary to bring the constituent elements to the proper oxidation state while maintaining the long mean free path necessary for MBE. Finally, composition control is crucial in order to repeatedly lay down exact "monolayers" of the desired composition. This report summarizes the highlight of demonstrating true single crystal growth of layered $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ compounds by MBE.

Prior epitaxial layers produced by both MBE and other deposition techniques have been oriented epitaxial layers. Although the crystallographic directions in the film are strongly influenced by the crystallographic form of the substrate (epitaxy), the presence of reflection twin boundaries or 90° rotation twin boundaries [Sleight] in both the $DyBa_2Cu_3O_{7-\delta}$ and $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ grown films distinguish these films from true single crystals. These reflection twin boundaries are not unlike the antiphase domains that occurred in early attempts to grow GaAs on Si. The solution to this problem was growth on intentionally misoriented substrates. Our superconductor work has always been done on carefully oriented substrates, however, we had some accidentally misoriented $SrTiO_3$. Growth on one of these accidentally misoriented $SrTiO_3$ (001) substrates, (misoriented about 3.8° → [110] and 0.9° → [110] as measured by the Laue method), produced the growth of the first true single crystal 2223 film by any technique.

The RHEED patterns observed immediately following growth are shown in Fig. 1. Figure 1(a) shows the RHEED pattern observed along the $SrTiO_3$ [110] azimuth, while Fig. 1(b) shows the RHEED pattern observed along the $SrTiO_3$ [110] azimuth. The RHEED patterns observed along the $SrTiO_3$ <110> azimuths are clearly different from each other. The closely spaced satellite streaks observed along the $SrTiO_3$ [110] azimuth indicate the lateral presence of the b axis and its superstructure, while the streaks observed along the $SrTiO_3$ [110] azimuth indicate the lateral presence of the a axis. In all our prior films, a superposition of these two patterns was observed along both perovskite <110> azimuths. Figure 1 shows the RHEED pattern observed along the $SrTiO_3$ [100] azimuth after growth.

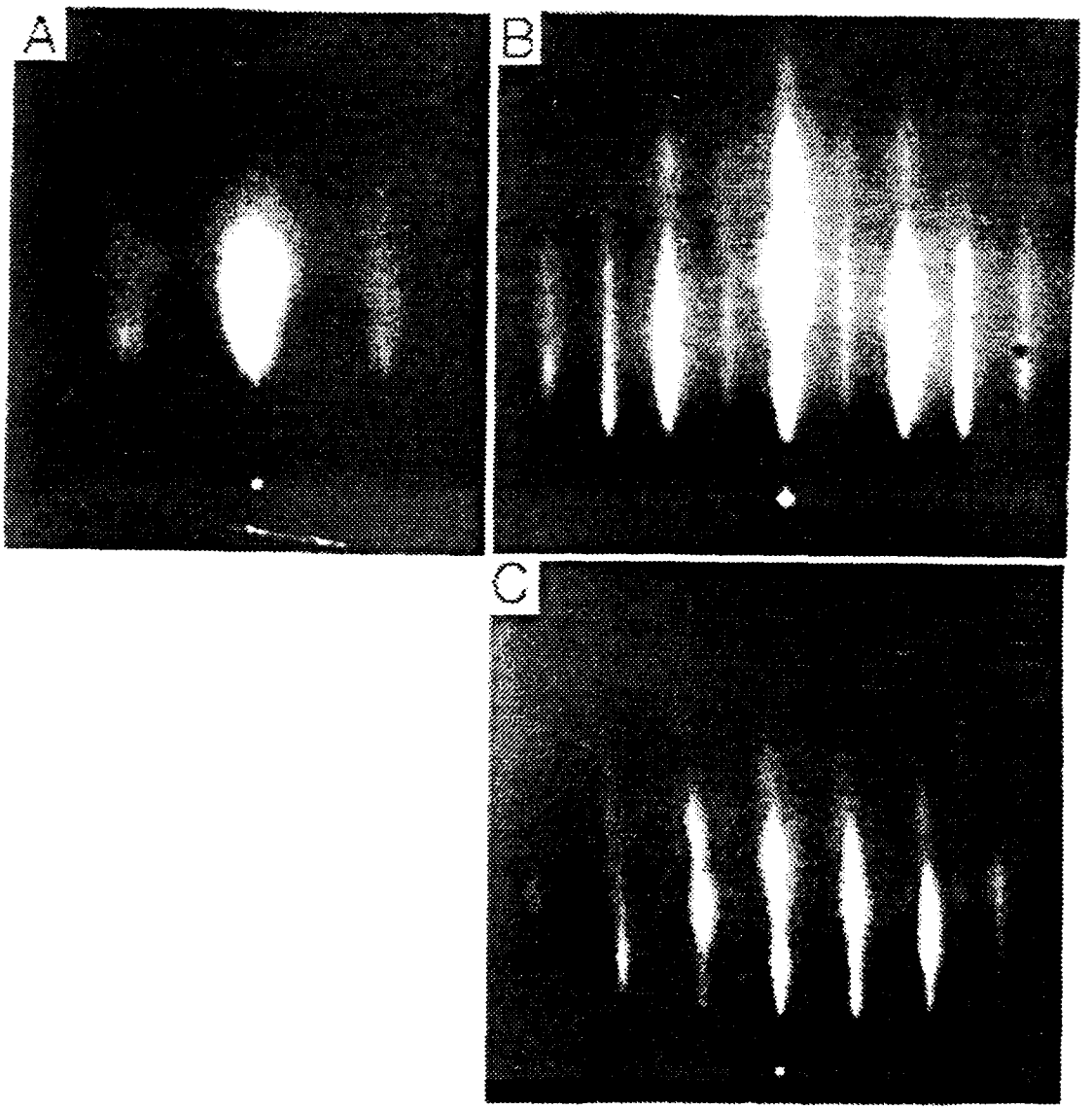


Figure 1 RHEED patterns observed after the growth of a 2223-like film on a misoriented $SrTiO_3$ (001) substrate. (Sample #399)
(a) $SrTiO_3$ [110] azimuth.
(b) $SrTiO_3$ [110] azimuth.
(c) $SrTiO_3$ [100] azimuth.

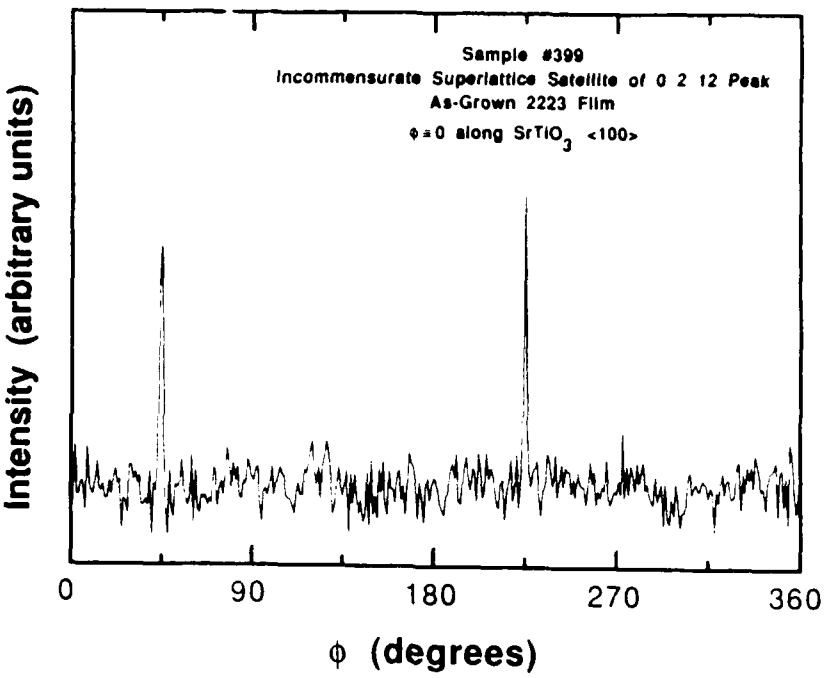


Figure 2 X-ray diffraction f scan of an incommensurate superlattice satellite peak of the 0212 peak of a 2223-like film grown on a misoriented $SrTiO_3$ {100} substrate. $\phi = 0$ was set parallel to $SrTiO_3$ <100>. This scan indicates that the b-axis of the 2223-like film runs up and down the steps of the misoriented substrate (45° and 225° peaks) but not laterally along them (no peak at 135° or 315°), indicating the absence of twin boundaries in the film. (Sample #399)

This film was also analyzed by x-ray diffraction to confirm the absence of reflection and rotation twin boundaries. Just as the incommensurate superstructure causes satellite streaks to occur in RHEED, it also produces satellite reflections in x ray diffraction. In particular the 0212 reflection of the 2223 phase has satellite peaks on either side of it along the b* reciprocal space axis, whereas the 2012 reflection does not have satellite peaks adjacent to it along the a* reciprocal space axis. Figure 2 shows the observed x ray diffraction pattern made by aligning the detector to a satellite reflection of the 0212 peak and then rotating the ϕ-axis of the 4-circle diffractometer around the [001] zone axis of the 2223 film. If the film contained rotation twin boundaries, then this scan would have contained a diffraction peak every 90° ((110) reflection twin boundaries would also lead to x-ray diffraction peaks about every 90° since the a and b axes have nearly identical length in these $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ materials). Instead, the observed x ray diffraction pattern contains only two peaks indicating that the incommensurate superlattice is aligned along only one of the <110> type $SrTiO_3$ surface directions. Specifically, the x ray data indicate that the b axis of the film runs up and down the substrate steps and not along the length of the substrate steps. If the high (distance from SrO to TiO_2 monolayers) $SrTiO_3$ {100} surface steps [Andersen] were equally spaced with a mean spacing equal to the incommensurate superlattice length, this would result in a misorientation of 4.3°, a value suggestively close to the misorientation observed in this sample.

The RHEED and x-ray diffraction results clearly demonstrate that this film grown on a misoriented $SrTiO_3$ {100} substrate does not contain reflection or rotation twin boundaries. Yet this diffraction data by itself is not sufficient to conclude that the film is a continuous single crystal. Real space crystallographic imaging (e.g. TEM or x-ray topography) is necessary to check for the presence of small angle grain boundaries or amorphous regions in the film. Although this work has not been done, grain boundaries or connected regions having different texture are not apparent by either optical or SEM microscopy. In addition, the TEM images of our twinned $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ films, which are grown under similar growth conditions, do not indicate the presence of boundaries other than twin boundaries in these films, supporting the conclusion that this film grown on a misoriented substrate is a true single crystal.

In conclusion, the ability of MBE to grow layered metastable $Bi_2Sr_2Ca_{n-1}Cu_nO_x$-like compounds in-situ is demonstrated. This is a major step in the development of a growth method capable of tailor-making layered combinations of perovskite-related compounds.

B. INVESTIGATION OF QUANTUM WELL STRUCTURES

1. Scientific Objectives

The objective of this project is to investigate heterojunction, quantum well and superlattice concepts and their application to new electronic devices with superior performance to devices based upon current semiconductor device principles. The small vertical dimensions which can now be readily achieved by Molecular Beam Epitaxy (MBE) make it possible to fabricate quantum well structures which are totally dominated by quantum mechanical effects. The properties of electron transport and storage in various regions of these quantum well structures are not well understood and their application to an entirely new generation of electron devices is in its infancy. The project will initially focus on the effects of doping on the electron transport in resonant tunneling diodes and new designs of double barrier resonant tunneling diodes to improve peak to valley current ratio and peak current density.

2. Summary of Research

Current resonant tunneling models ignore effects of accumulation layers, spacers, etc., in the cathode region. We have focused initial efforts on understanding the role of the cathode region and its role in optimizing device design. Goodhue et al [Goodhue] were the first to begin bandgap engineering to optimize RTD performance. They observed a PVCR of 3.5 (10.0) at 300K (77K) in an AlAs/GaAs DBRTD. Recently, Huang et al [Huang] used a two step spacer structure in DBRTDs to improve the PVCRs to 3.6 (21.7) at 300K

(77K) in an AlAs/GaAs superlattice barrier DBRTDs and to 3.9 (14.3) at 300K (77K) in an alloy barrier DBRTD with x=0.42 (where x is Al composition). Lear [Lear] was the first to really focus on the role of the cathode region. They used an InGaAs well in the cathode of an AlAs/GaAs DBRTD and observed a PVCR as high as 4.8 at room temperature. Based upon our work on the role of X valley tunneling, we began to investigate the role of wider, low energy "chair" barriers on both X valley tunneling and tunneling form the accumulation layer in the cathode. Record values of PVCR of 6.0 were observed for DBRTDs in the GaAs/AlGaAs system [Cheng]. These improvements in RTD design should enhance the performance of millimeter wave DBRTDs as well as devices into which DBRTDs have also been incorporated, such as bipolar transistors [Futatsugi] and three terminal quantum wire structures [Luryi]. The design and performance of the novel chair barrier structure which has led to this record performance is described in this section.

Three samples were grown consecutively on n+ GaAs (100) substrates at 600°C by molecular beam epitaxy in a Varian GEN II system. In sample A, the AlAs/GaAs/AlAs double barrier structure was grown on top of a 5000Å thick, $2x10^{18}cm^{-3}$ Si doped buffer layer. The thickness of both AlAs barriers is 20Å. The GaAs well width is 50Å. The barriers and the well are undoped. In sample B, an undoped 4 monolayer $Al_{0.14}Ga_{0.86}As$ chair barrier was grown before the growth of the AlAs/GaAs/AlAs double barrier structure. In sample C, an undoped four monolayer spatially separated, real $Al_{0.14}Ga_{0.86}As$ barrier was grown before the growth of the second step spacer layer at the bottom.

The rest of the structure of samples B and C is identical to that of sample A. A schematic diagram of the structures and their conduction band profiles are shown in Fig. 3(a). By comparing the results observed from sample A and B, the effects of the $Al_{0.14}Ga_{0.86}As$ chair barrier can be studied. The results observed from sample C demonstrate the effects of the same height, but spatially separated, real $Al_{0.14}Ga_{0.86}As$ barrier.

In order to study the effects of the AlGaAs chair more thoroughly, two more RTDs were grown on semi-insulating substrates by MBE at a later time. The double barrier structures were identical to samples A, B and C. In sample D, the AlAs/GaAs/AlAs double barrier structure was grown on top of a 5000Å thick, $2x10^{18}cm^{-3}$ Si doped buffer layer. A four monolayer $Al_{0.25}Ga_{0.75}As$ chair barrier was grown before the growth of the AlAs/GaAs/AlAs double barrier structure. The structure of sample E was identical to the structure of sample D except that Al alloy composition of the four monolayer chair barrier was increased to $Al_{0.4}Ga_{0.6}As$. Samples D and E were grown consecutively. The entire structures were grown at 600°C substrate temperature except the final nonalloyed ohmic contact layers, which were grown at 400°C. The schematic diagrams of the structures and

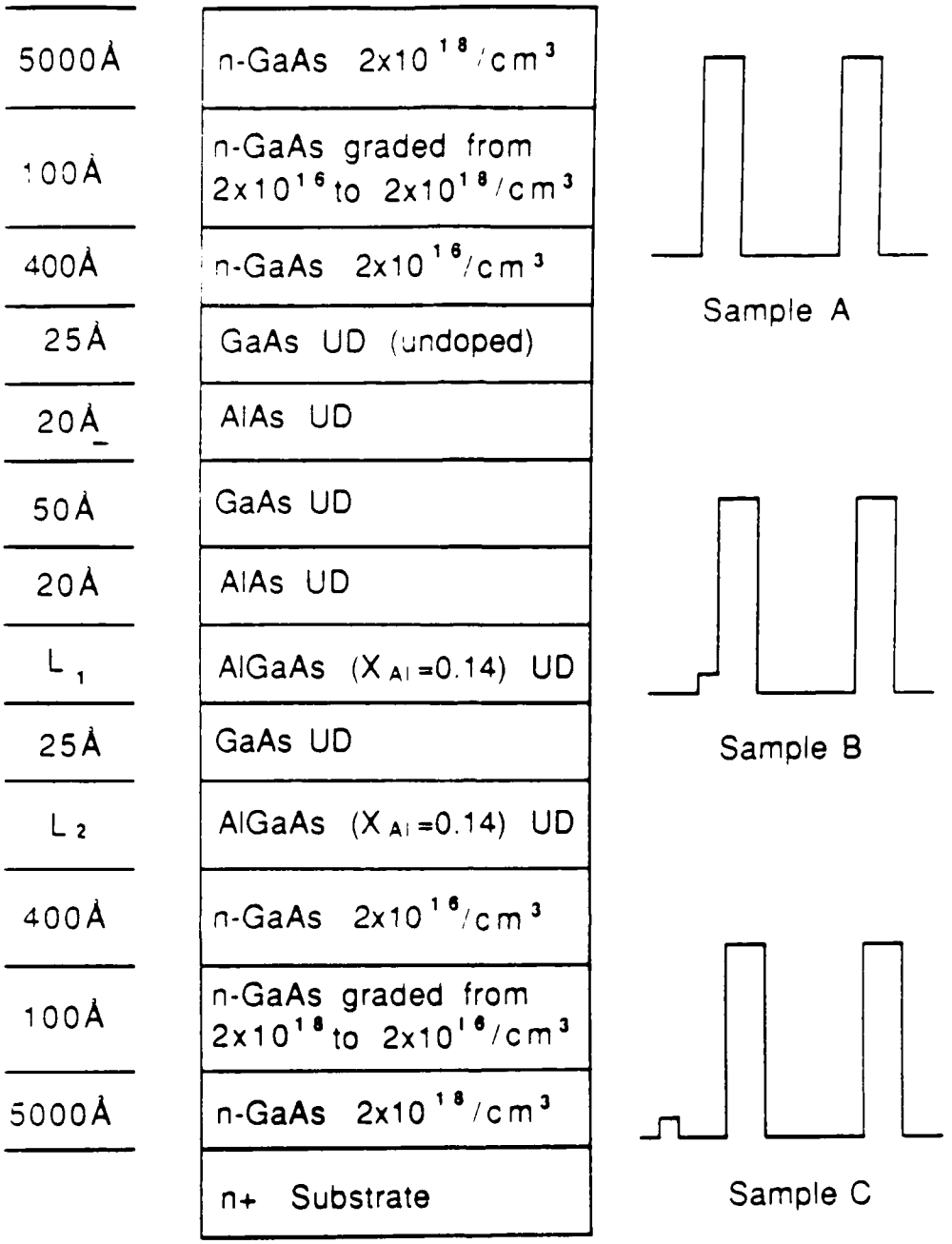
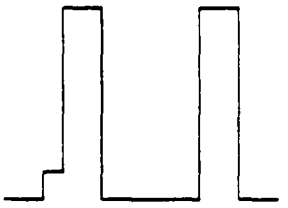


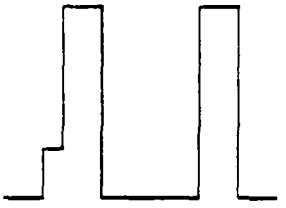
Figure 3(a) Schematic diagrams of the structures and conduction band profiles of samples A, B and C. In sample A, $L_1 = L_2 = 0$; In sample B, $L_1 = 4$ monolayers, $L_2 = 0$; In sample C, $L_1 = 0$, $L_2 = 4$ monolayers.

conduction band profiles of samples D and E are shown in Fig. 3(b). By comparing the structures of samples B, D and E, we see that the active structures (spacers, barriers and well) of the three samples are identical. The only difference is the Al and Ga composition of the AlGaAs chair barrier in the cathode. The differences in the substrate type and top contacting layer between samples B, D and E should not significantly effect the performance of the DBRTDs. By comparing samples B, D and E, effects of the height of AlGaAs chair barrier on the performance of DBRTDs can be studied.

600A	Non-alloyed Contact
2500Å	n-GaAs $2x10^{18}/cm^3$
100Å	n-GaAs graded from $2x10^{16}$ to $2x10^{18}/cm^3$
400Å	n-GaAs $2x10^{16}/cm^3$
25Å	GaAs UD (undoped)
20Å	AlAs UD
50Å	GaAs UD
20Å	AlAs UD
4 ML	$Al_xGa_{1-x}As$ UD
25Å	GaAs UD
400Å	n-GaAs $2x10^{16}/cm^3$
100Å	n-GaAs graded from $2x10^{18}$ to $2x10^{16}/cm^3$
5000Å	n-GaAs $2x10^{18}/cm^3$
	SI Substrate



Sample D



Sample E

Figure 3(b) Schematic diagrams of the structures and conduction band profiles of samples D and E. In sample D, x = 0.25 and in sample E, x = 0.4.

Figures 4(a) and 4(b) show typical I-V characteristics of diodes on samples A and B at room temperature. The forward bias direction is defined as electrons moving from the bottom to top of the DBRTD (the chair barrier on the cathode side). The room temperature resonant tunneling data measured from more than one hundred, 7x7 mm diodes on A and B samples is summarized in Table 1. The average PVCRs observed in sample A was 4.1 in both forward and reverse bias directions. The highest PVCR observed in sample A was 4.2 in both bias directions. The excellent symmetry in the I-V characteristics of sample A suggests that the structure of the sample is quite symmetric. The slight asymmetry is likely

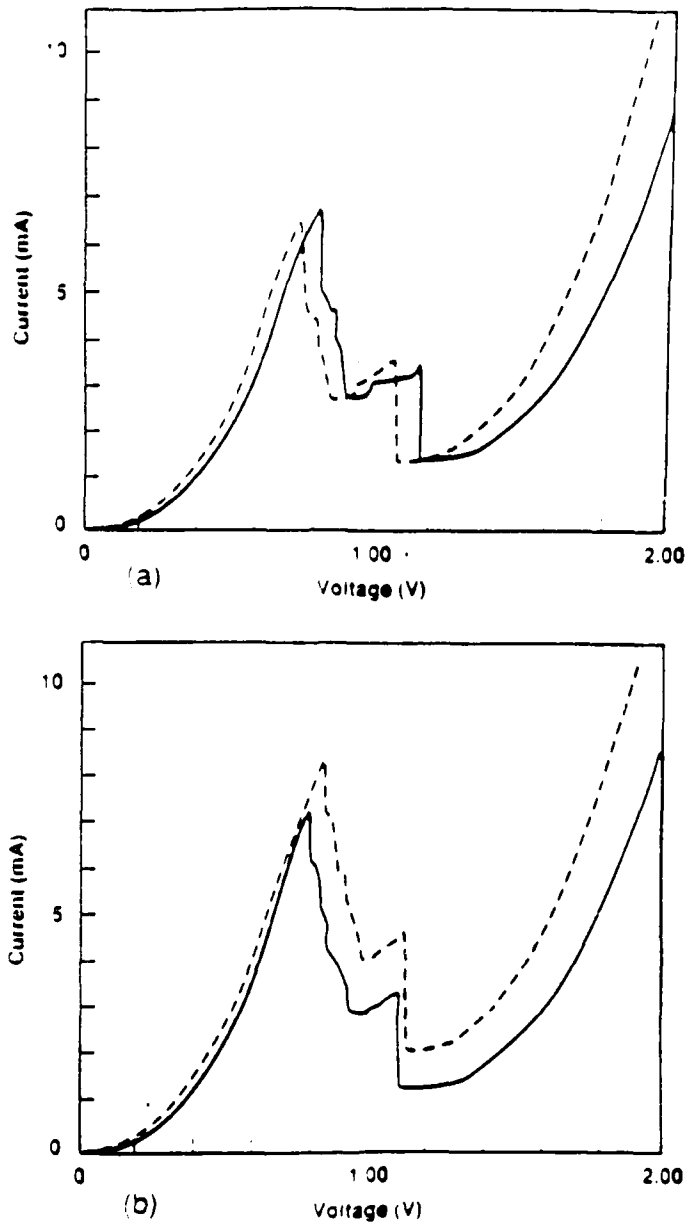


Figure 4(a) and 4(b), current-voltage characteristics of samples A and B at room temperature, respectively. The solid and dotted lines are the I-V curves under forward and reverse bias, respectively.

caused by the inferior inverted interface morphology of the quantum well and contact region [Shewchuck]. The average PVCR observed in sample B was 5.0 and 3.7 under forward and reverse bias, respectively. The highest PVCR observed in sample B was 5.1 and 3.7 under forward and reverse bias, respectively. In sample B, both peak and valley currents under forward bias are smaller than those under reverse bias. The I-V measurements have also been made at 77K. PVCRs of 12.0 and 11.7 were observed in sample A under forward and reverse bias, respectively. PVCRs of 13.7 and 9.1 were observed in sample B under forward and reverse bias, respectively.

Sample	A		B	
Bias direction	Forward	Reverse	Forward	Reverse
Average PVCR	4.1	4.1	5.0	3.7
Highest PVCR	4.2	4.2	5.1	3.7
I_{Peak} (mA)	6.54±0.02	6.22±0.03	7.21±0.14	8.22±0.13
I_{Valley} (mA)	1.58±0.01	1.52±0.01	1.44±0.03	2.26±0.04
V_{Peak} (V)	0.86±0.01	0.78±0.01	0.79±0.02	0.83±0.01
V_{Valley} (V)	1.22±0.01	1.12±0.01	1.18±0.01	1.20±0.003

Table 1. The resonant tunneling data for 7x7 mm diodes on samples A and B at 300K.

The $Al_{0.14}Ga_{0.86}As$ chair barrier can decrease the coherent tunneling current in the valley because the bottom of the first tunneling barrier is thicker. The probability of the electrons in the accumulation layer tunneling through the double barrier structure is much smaller because of the presence of the chair barrier. Electron tunneling through the X valley can also be significantly decreased by the chair barrier because the X valley in the chair barrier is 0.42eV, which is much higher than the X valley in AlAs barrier (E_X=0.19eV). The value of the X valley energies are calculated from the bandgap data in Adachi's Review [Adachi] and the band lineup is obtained by assuming $\Delta E_V = 0.55X_{Al}$ (eV) [Batey]. It can be seen from Table 1 that although both the peak and valley currents in sample B are reduced by a similar amount (the peak and valley currents are 1.01mA and 0.82mA, respectively, they are smaller under forward bias than that under reverse bias), the valley current under forward bias is about 37% smaller than that under reverse bias and the peak current is only about 12% smaller. The average PVCR of sample B is improved from 3.7 under reverse bias to 5.0 under forward bias. The advantage of using this $Al_{0.14}Ga_{0.86}As$ chair barrier is that the PVCR can be significantly improved while the peak current density decrease only slightly.

It can be seen from Table 1 that the peak current under forward bias in sample B is about 10% higher than that in sample A. This contradicts our calculation which shows that the peak current under forward bias in sample B is predicted to be smaller than that of sample A. It can also be seen from Table 1 that in sample B, the peak current under forward bias is smaller than that under reverse bias. This shows that the $Al_{0.14}Ga_{0.86}As$ chair barrier in the cathode decreases the peak current. From our calculation we find that a one monolayer fluctuation in AlAs barrier thickness can cause more than 300% variation in resonant tunneling peak current. We believe that the increase in peak current under forward bias in sample B compared to sample A is caused by such thickness fluctuations during growth.

Sample	C	
Bias direction	Forward	Reverse
Average PVCR	3.7	4.7
Highest PVCR	3.7	4.8
Peak current (mA)	4.66±0.04	8.89±0.08
Valley current (mA)	1.28±0.01	1.88±0.01
Peak voltage (V)	0.68±0.02	0.81±0.03
Valley voltage (V)	0.99±0.01	1.17±0.01

Table 2. The resonant tunneling data for 7x7 mm diodes on sample C at 300K.

A summary of the room temperature resonant tunneling data is presented in Table 2. A PVCR as high as 4.8 was observed under reverse bias when the $Al_{0.14}Ga_{0.86}As$ barrier was in the anode and a PVCR of 3.7 was observed under forward bias when the $Al_{0.14}Ga_{0.86}As$ barrier was in the cathode. The peak current under reverse bias is almost twice as large as that under forward bias, while the valley current under reverse bias is only about 50% larger than that under forward bias.

The room temperature resonant tunneling data and their standard deviations measured from more than 200 diodes on samples D and E are summarized in Table 3. The dimension of the diodes on samples D and E was 8x10 mm. Average PVCRs observed on samples D and E under forward bias were 5.8 and 5.6, respectively. The highest PVCRs observed on samples D and E were 6.0 and 5.9 under forward bias, respectively. The PVCR of 6.0 observed on sample D is the highest PVCR observed to date at room temperature in AlGaAs/GaAs DBRTD. Average PVCRs observed on samples D and E under reverse bias were 3.5 and 2.7, respectively. Figure 5 shows the values of the average PVCRs measured from samples A, B, D and E as a function of the Al composition in the chair barrier. As can be seen in Fig. 5, the PVCR under forward bias reaches a maximum when the $Al_{0.25}Ga_{0.75}As$ chair barrier is used, while the PVCRs under reverse bias monotonically decrease.

Sample	D (25% Al)		E (40% Al)	
Bias direction	Forward	Reverse	Forward	Reverse
Average PVCR	5.8±0.1	3.5±0.1	5.6±0.2	2.7±0.1
Highest PVCR	6.0	3.6	5.9	2.8
I_{Peak} (mA)	8.46±1.24	12.3±1.45	4.37±0.94	8.46±1.53
I_{Valley} (mA)	1.46±0.20	3.55±0.41	0.78±0.15	3.19±0.53
V_{Peak} (V)	0.82±0.09	1.14±0.13	0.65±0.07	1.14±0.14
V_{Valley} (V)	1.00±0.04	1.30±0.06	0.91±0.04	1.36±0.09

Table 3. The resonant tunneling data for 8x10 mm diodes on sample D and E at 300K.

As we have discussed before, the AlGaAs chair barrier in the cathode can decrease both the tunneling current from the accumulation layer and the X valley tunneling current, so that the PVCRs of DBRTDs with chair barriers under forward bias are improved, compared to standard DBRTDs. As the Al composition in AlGaAs chair barrier increases, the Γ point of the chair barrier increases so that the tunneling current from accumulation layer continues to decrease. However, the X point of the chair barrier decreases as the Al composition increases so that the X valley tunneling current increases. The maximum PVCR should occur when the sum of the tunneling current from the accumulation layer and the X valley tunneling current is minimized. As can be seen in Fig. 5, the maximum PVCR is observed when the $Al_{0.25}Ga_{0.75}As$ chair barrier is used. When the Al composition in the chair barrier is increased from 0 to 25% (The Γ point of the chair barrier is increased from 0 to 174meV and the X point of the chair barrier is decrease from 476meV to 379meV), the average PVCR increases from 4.1 to 5.8. When the Al composition in the chair barrier reaches 40% (The Γ point of the chair barrier is 279meV and the X point of the chair barrier is 329meV), the average PVCR decreases to 5.6 from 5.8 observed on the $Al_{0.25}Ga_{0.75}As$ chair barrier sample. We conclude from the above that the tunneling current from the accumulation layer dominates the valley current when the Al composition in the chair barrier is less than 25%. When the Al composition in the chair barrier is greater than 40%, the X valley tunneling current starts to dominate.

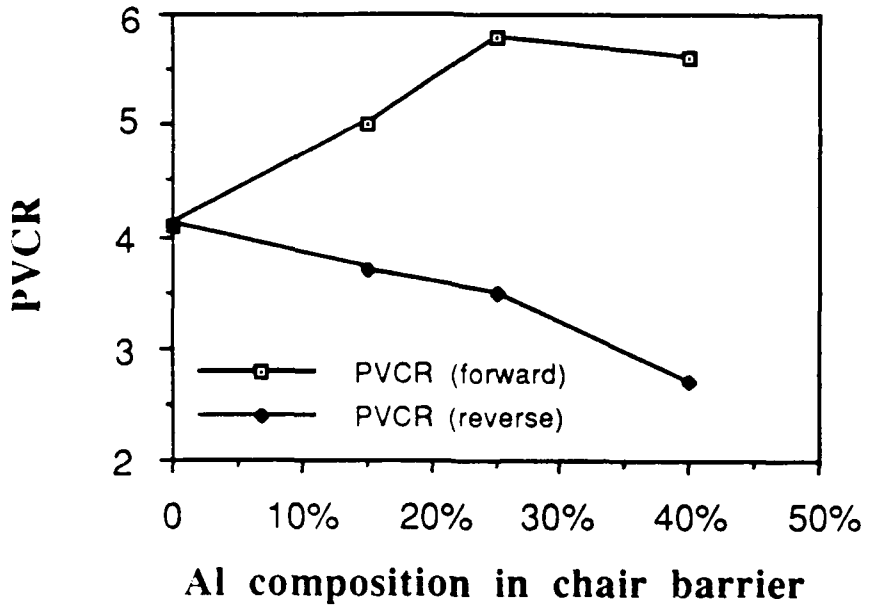


Figure 5 The dependence of PVCRs on Al composition in chair barrier RTDs.

In conclusion, we have demonstrated an improved design for the DBRTD using an AlGaAs chair barrier. The highest room temperature PVCR for an AlGaAs/GaAs DBRTD to date, 6.0, is observed in the chair barrier structure with an $Al_{0.25}Ga_{0.75}As$ chair barrier on the cathode side. PVCRs as high as 5.1 and 5.9 have been observed in DBRTDs with $Al_{0.14}Ga_{0.86}As$ and $Al_{0.4}Ga_{0.6}As$ chair barriers, respectively. We attribute the improvement in PVCR to the reduction of two valley current components, tunneling current from the accumulation layer and the X valley tunneling current , by the AlGaAs chair barrier. The maximum PVCR occurs when the sum of the two currents is minimized. It is found that tunneling current from the accumulation layer dominates the valley current when the Al composition in the chair barrier is less than 25%. When the Al composition in the chair barrier is greater than 40%, the X valley tunneling cur ent starts to dominate.

It has been difficult to simultaneously achieve both high peak current density and high PVCR. Since he $Al_{0.14}Ga_{0.86}As$ chair barrier structure can significantly improve the PVCR while only slightly reducing the peak current density, the $Al_{0.14}Ga_{0.86}As$ chair barrier structure can be incorporated into high current density diodes to improve their PVCR. For other RTD applications requiring high PVCR, optimized chair barrier structures such as $Al_{0.25}Ga_{0.75}As$ chair barrier should be used. Although the chair barrier experiment was done in the AlGaAs/GaAs system, the chair barrier should also improve the PVCR of RTDs based on the InGaAs system.

JSEP SUPPORTED DISSERTATIONS

1. Darrell G. Schlom, "Molecular Beam Epitaxial Growth of Cuprate Superconductors and Related Phases", Ph.D. Dissertation, Stanford University, Stanford, CA, June, 1990.
2. Peng Cheng, "Novel Tunneling Barrier Designs for Resonant Tunneling Diodes", Ph.D. Dissertation, Stanford University, Stanford, CA, January, 1991.

JSEP SUPPORTED PUBLICATIONS

1. E. S. Hellman, D. G. Schlom, A. F. Marshall, S. K. Streiffer, J. S. Harris, Jr., M. R. Beasley, J. C. Bravman, T. H. Geballe, J. N. Eckstein and C. Webb, "Phase Characterization of Dysprosium Barium Copper Oxide Thin Films Grown on Strontium Titanate by Molecular Beam Epitaxy," *J. Mater. Res.*, **4**, (3), pp. 476-495, May/Jun 1989.
2. J. S. Harris, Jr., J. N. Eckstein, E. S. Hellman and D. G. Schlom, "MBE Growth of High Critical Temperature Superconductors," *J. of Crystal Growth* **95**, pp. 607-616, 1989.
3. P. Cheng, B. G. Park, S. D. Kim and J. S. Harris, Jr., "The X-Valley Transport in GaAs/AlAs Triple Barrier Structures" *J. Appl. Phys.* **65**, (12), June 1989.
4. J. N. Eckstein, J. S. Harris, Jr., D. G. Schlom, I. Bozovic, K. E. von Dessoneck and Z. J. Chen, "Development of Molecular Beam Epitaxial Growth of High Temperature Superconducting Compounds," *International Superconductivity Electronics Conf.*, Tokyo, Japan, June 1989.
5. P. Cheng and J. S. Harris, Jr., "The Effect of Si Doping in AlAs Barrier Layers of AlAs-GaAs-AlAs Double Barrier Resonant Tunneling Diodes," *Appl. Phys. Lett.* **55**, (6), August 1989.
6. S. Y. Chou, D. R. Allee, R. F. W. Pease and J. S. Harris, Jr., "New Lateral Resonant Tunneling FETs Fabricated Using Molecular Beam Epitaxy and Ultra-High Resolution Electron Beam Lithography", *Proceedings of 16th International Symposium on GaAs and Related Compounds*, Karuizawa, Japan, pp. 875-879, September 1989.
7. D. G. Schlom, J. N. Eckstein, I. Bozovic, A. F. Marshall, J. T. Sizemore, Z. J. Chen, K. E. Von Dessonneck, J. S. Harris, Jr. and J. C. Bravman, "Molecular Beam Epitaxy of Layered Bi-Sr-Ca-Cu-O Compounds," *Proceedings of Fall Materials Research Society Symposium M: High-Temperature Superconductors*, November 1989.
8. D. G. Schlom, A. F. Marshall, J. T. Sizemore, Z. J. Chen, J. N. Eckstein, I. Bozovic, K. E. von Dessonneck and J. S. Harris, Jr., "Molecular Beam Epitaxial Growth of Layered Bi-Sr-Ca-Cu-O Compounds," *Jrnl. Cryst. Gwth.*, **102**, pp. 361-375, February 1990.

9. D. G. Schlom, J. N. Eckstein, I. Bozovic, A. J. Chen, A. F. Marshall, K. E. von Dessonneck, J. S. Harris, Jr., "Molecular Beam Epitaxy-a Path to Novel High T_c Supercondonductors," *Proceedings of Growth of Semiconductor Structures and High-T_c Thin Films on Semiconductors*," SPIE, **1285**, pp. 234-247, March 1990.
10. Peng Cheng and James S. Harris, Jr., " Improved Design of AlAs/GaAs Resonant Tunneling Diodes", *proceedings SPIE Conference - "Quantum Well and Superlattice Physics III"*, **1283**, pp. 353-358, March 1990.
11. J. H. Kim, I. Bozovic, D. B. Mitzi and A. Kapitulnik and J. S. Harris., Jr., "Optical Anisotropy of $Bi_2Sr_2CaCu_2O_8$," *Phys. Rev. B*, **41**, 10, April 1990.
12. P. Cheng and J. S. Harris, Jr., "Improved Design of AlAs/GaAs Resonant Tunneling Diodes", *Appl. Phys. Lett.* **56** (17) April 23, 1990.
13. K. Kojima, D. G. Schlom, K. Kuroda, M. Tanioku, K. Hamanaka, J. N. Eckstein and J. S. Harris, Jr., "Superstructure in Thin Films of Bi-Based Compounds on MgO," *Japanese Jrnl of Appl. Phys*, **29**, 9, pp. L1638-L1641, September 1990.
14. J. N. Eckstein, I. Bozovic, D. G. Schlom and J. S. Harris, Jr., "Growth of untwinned $Bi_2Sr_2Ca_2Cu_3O_x$ Thin Films y Atomically Layered Epitaxy," *Appl. Phys. Lett.* **57**, pp 1049-1051. September 1990.
15. D. G. Schlom, A. F. Marshall, J. S. Harris, Jr., I. Bozovic and J. N. Eckstein, "Growth of Metastable Phases and Superlattice Structures of Bi-Sr-Ca-Cu-0 Compounds by an Atomic Layering MBE Technicque", *Proceedings 3rd Int'l. Symp. on Superconductivity*, Sendai, Japan, November 1990.
16. D. R. Allee, S. Y. Chou, J. S. Harris, Jr., and R. F. W. Pease, " Resonant Tunneling of 1-Dimensional Electrons Across an Array of 3-Dimensionally Confined Potential Wells," *Superlattices and Microstructures*, **7**, (2), pg. 131-134, 1990.

JSEP SUPPORTED PRESENTATIONS

1. S. Y. Chou, D. R. Allee, R. F. W. Pease and J. S. Harris, Jr., "Quantum interference Devices Fabricated Using Molecular Beam Epitaxy and Ultra-High Resolution Electron Beam Lithography" *Device Research Conference*, IEEE, MIT Cambridge, MA June 1989.
2. S. Y. Chou, D. R. Allee, R. F. Pease and J. S. Harris Jr., "New Lateral Resonant Tunneling FETs Fabricated Using Molecular Beam Epitaxy and Ultra-High Resolution Electron Beam Lithography"*16th International Symposium on GaAs and Related Compounds*, Kuruizawa, Japan, Sept. 1989.
3. J. S. Harris, "Growth of High T_c Superconductors by MBE", *AGARD Workshop*, Trondheim, Norway, September 1989. **(Invited)**.
4. J. S. Harris, "Multi-Material Electronic Structures", *AGED Group B STAR Review*, Crystal City, VA, October 1989 **(Invited)**.
5. D. G. Schlom, J. N. Eckstein, I. Bozovic, A. F. Marxhall, J. T. Sizemore, Z. J.

Chen, K. E. von Dessonneck, J. S. Harris, Jr., and J. C. Bravman, "Molecular Beam Epitaxy of Layered Bi-Sr-Ca-Cu-O Compounds", *Fall Materials Research Society Symposium M: High-Temperature Superconductors, Boston*, Nov. 1989.

6. D. G. Schlom, J. N. Eckstein, I. Bozovic, Z. J. Chen, A. F. Marshall, K. E. von Dessonneck, J. S. Harris, Jr., "Molecular Beam Epitaxy - a Path to Novel High T_c Superconductors," *SPIE Conference: Growth of Semiconductor Structures and High-T_c Thin Films on Semiconductors*, San Diego, March 1990 **(Invited)**.
7. P. Cheng and J. S. Harris, Jr., "Improved Design of AlAs/GaAs Resonant Tunneling Diodes", SPIE Conference: Quantum Well and Superlattice Physics III, San Diego, CA March 1990.
8. D. G. Schlom, J. N. Eckstein, K. E. von Dessonneck, Z. J. Chen, I. Bozovic, J. Sizemore, C. Webb, F. Turner, J. S. Harris, Jr., J. C. Bravmen, M. R. Beasley, and T. H. Geballe, "Molecular Beam Epitaxy of Layered Bi-Sr-Ca-Cu-O Compounds," Spring Materials Research Society Symposium on *High-Temperature Superconductors*, San Diego, CA, April 1990.
9. J. N. Eckstein and I. Bozovic, D. G. Schlom, Z. J. Chen, and J. S. Harris, "In-Situ Growth of Single Crystal $Bi_2Sr_2Ca_nCu_{n+1}O_x$ Thin Films by Atomically Layered Epitaxy", *1990 Electronic Materials Conference*, UCSB, Santa Barbara, CA, June 1990.
10. J. N. Eckstein, I. Bozovic, D. G. Schlom, and J. S. Harris, Jr., "Growth of Superconducting $Bi_2Sr_2Ca_{n-1}Cu_nO_x$ Thin Films by Atomically Layered Epitaxy," *VI Int'l MBE Conference*, UCSD, San Diego, CA, August 1990.
11. D. G. Schlom, A. F. Marshall, J. S. Harris, Jr., I. Bozovic, J. N. Eckstein, "Growth of Metastable Phases and Superlattice Structures of Bi-Sr-Ca-Cu-O Compounds by an Atomic Layering MBE Technique" *3rd Int'l Symp. on Superconductivity*, Sendai, Japan, November 6-9, 1990. **(Invited)**
12. D. G. Schlom, A. F. Marshall, J. S. Harris, Jr., I. Bozovic, J. N. Eckstein, "Growth of Metastable Phases and Superlattice Structures of Bi-Sr-Ca-Cu-O Compounds by an Atomic Layering MBE Technique," *Symposium of Superconductivity of the Japan Society of Powder and Powder Metallurgy*, November 15-16, 1990, Kyoto, Japan **(Invited)**.

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Unit: 2

TITLE: Physics and Applications of Ultra-Small, High-Temperature Superconductors

SENIOR INVESTIGATORS: R. F. W. Pease

RESEARCH STUDENTS: B. Boyer and H. Liu

Scientific Objectives

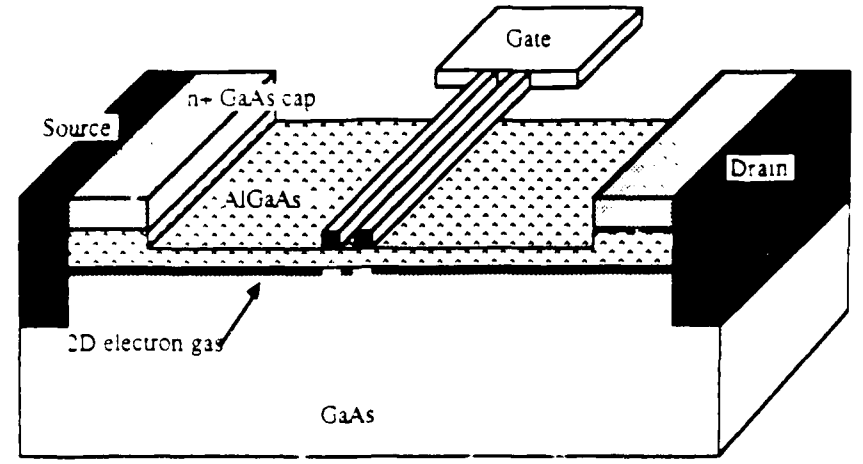
The overall objectives of this program are to investigate opportunities for new devices whose operation depends on quantum mechanical effects associated with the ultrasmall (<100nm) nature of these devices. Obviously we hope to realize device concepts that promise superior performance than that achieved by devices based on current principles. Even if that desirable end is not achieved we should in any case be in a position to optimize the design of devices employing lateral features below 100 nm when our ability to fabricate them moves beyond the laboratory into manufacturing. During the present reporting period we have had two specific goals: to conclude the first project on lateral quantum well devices employing compound 3-5 semiconductors and to initiate the project in ultrasmall superconducting structures.

Progress for the period 1 July 1989 to 31 June 1990

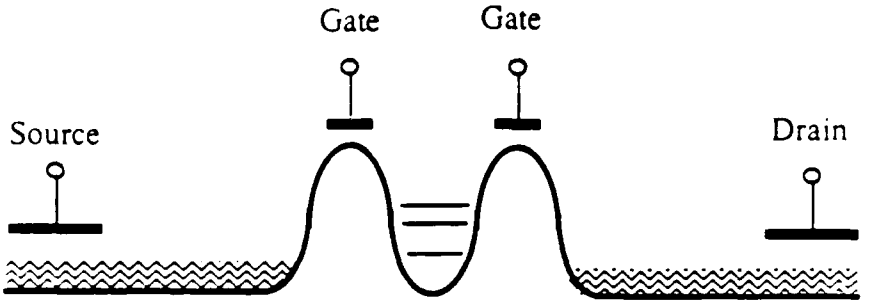
1. Ultrasmall Lateral Quantum-well Devices

During this reporting period the project on lateral quantum well devices has been successfully concluded with the publication of D. R. Allee's Ph.D. dissertation and accompanying articles [Allee].

The main conclusions were reported in last year's report. Further work in this area has been restricted to a more elaborate calculation (by H. Liu) of the potential barrier seen by the carriers in a two-dimensional electron gas (2DEG) underneath a one-dimensionally periodic, multi-electrode gate. In particular, this calculation led to improved understanding about the optimum geometry of the electrode structure needed to maximize the height of the potential barriers and the magnitude of the resulting oscillations in the conductance versus gate voltage curves at low temperatures (Fig. 1).



a)



b)

Figure 1a Structure of multi-gate device.

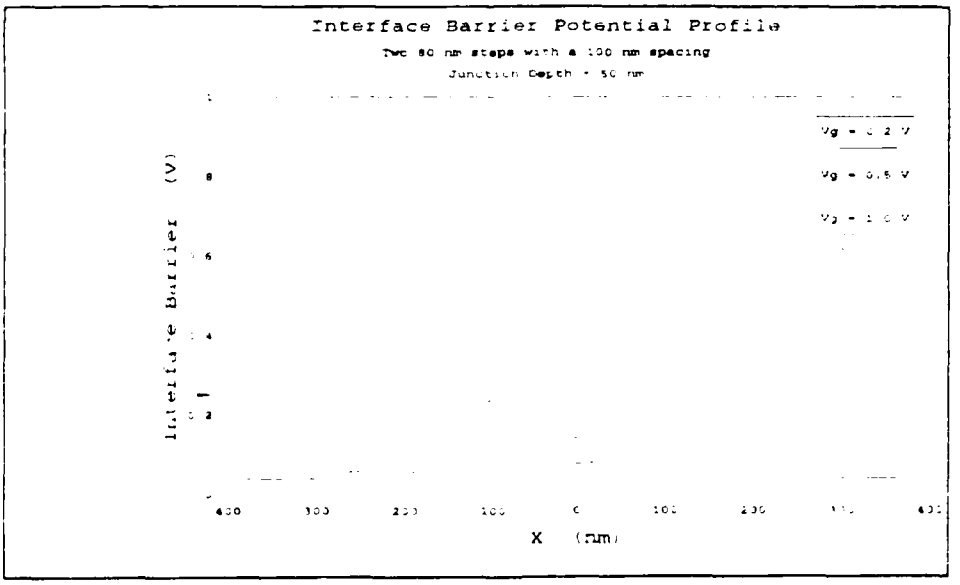


Figure 1b Calculated profiles of potential (conduction band edge) seen by a carrier in the 2DEG just underneath the AlGaAs layer. This calculation takes into account the screening by the carriers in the structure.

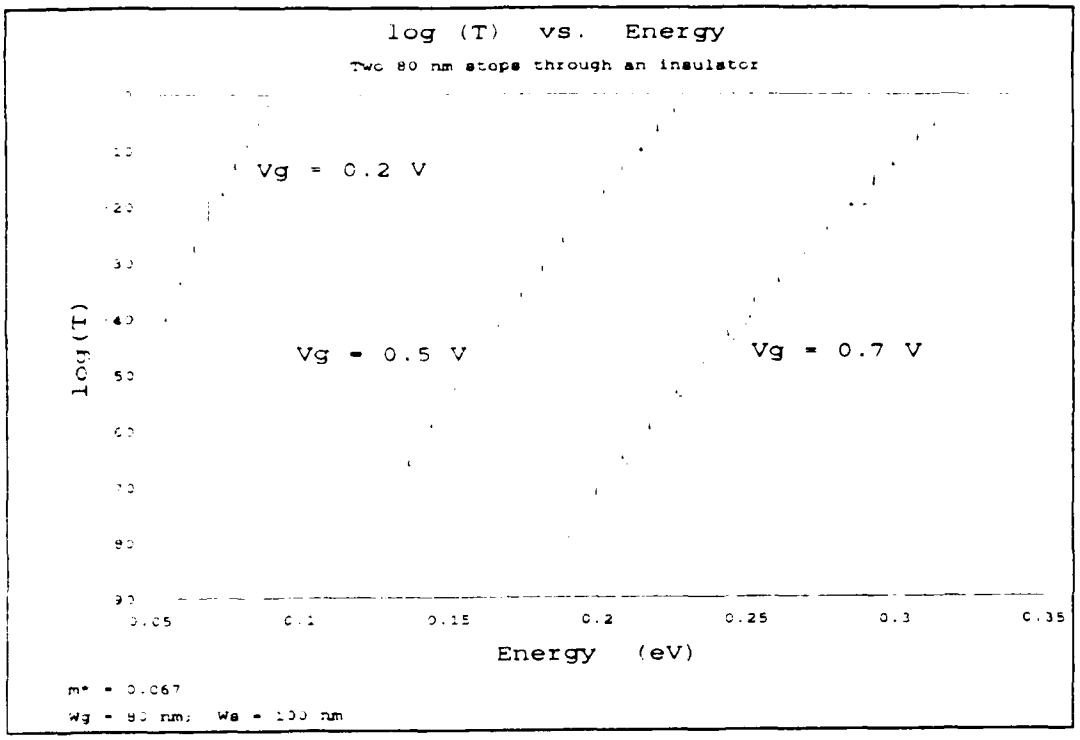


Figure 1c The conductance/Vgs curves that should result from the optimized structure.

2. Ultrasmall Superconducting Structures and Devices

Devices based on weak links in metallic superconductors were originally demonstrated many years ago [Lee], [Schwartz]. Lateral devices and structures made with nanometer-scale fashioning of metallic superconductors has also been demonstrated [Feuer]. This project is to investigate how best to use these techniques on high-temperature superconductors. The first phase of this project has been to build up a fabrication technology for this new class of materials and to demonstrate that superconducting properties are not adversely affected by the techniques employed. During this reporting period substantial progress has been made and superconducting submicron weak link structures in YBCO have been demonstrated as described below.

The material used was YBCO grown on MgO substrates by a 90° off-axis sputtering technique. The substrate temperature during growth was 720C. This process produces in-situ superconducting thin films. In the near future, other substrates such as $LaAlO_3$ or sapphire will be utilized because of their superior thermal and microwave properties.

The patterning technique has been electron beam lithography employing an SEM (Hitachi S800) interfaced to a PC-based ELPHY I pattern generator. This SEM was chosen because of its high resolution and very intense beam (hundreds of pA into a spot size less than 4 nm in diameter). These characteristics give us the flexibility to consider patterning techniques which have the highest resolutions ever reported (e.g. the 20 nm features Muray and Isaacson obtained in aluminum fluoride) [Muray]. A disadvantage of this SEM for fabrication is its field emission electron gun, which exhibits beam current drifting over periods greater than 10 minutes. Fortunately, the pattern for a single device is simple enough that the total exposure time should be a few minutes at most.

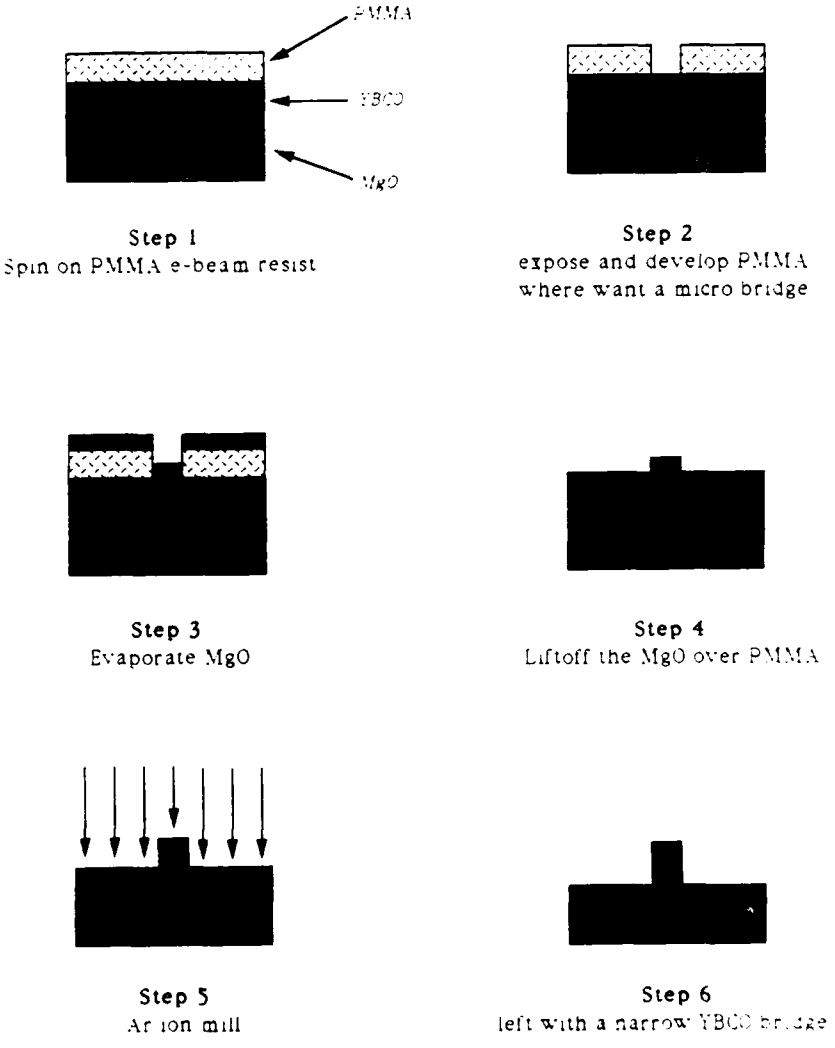


Figure 2 High resolution lithography process sequence used in the fabrication of submicron superconducting junctions.

Our early experiments in high resolution patterning of YBCO films were attempts to damage YBCO using the intense beam of the SEM. With the beam energies available to us (5 - 25 keV), we were not able to obtain satisfactory levels of damage to pattern a film. So, we have resorted to more conventional approaches. One sequence is shown in Fig. 2 and employs an intermediate film of MgO to act as an ion milling mask. This sequence has not yet yielded structures as small as 160 nm so further improvement is required.

With this process sequence we have fabricated weak link structures in YBCO films and have shown that these possess superconducting properties. Top and side views of the structures built, an SEM view and I/V curves of the resulting junction are shown in Fig. 3.

This work has been carried out in collaboration with members of the Ginzton Laboratory (Geballe, Beasley, Kapitulnik groups) who have provided the films and assistance in testing.

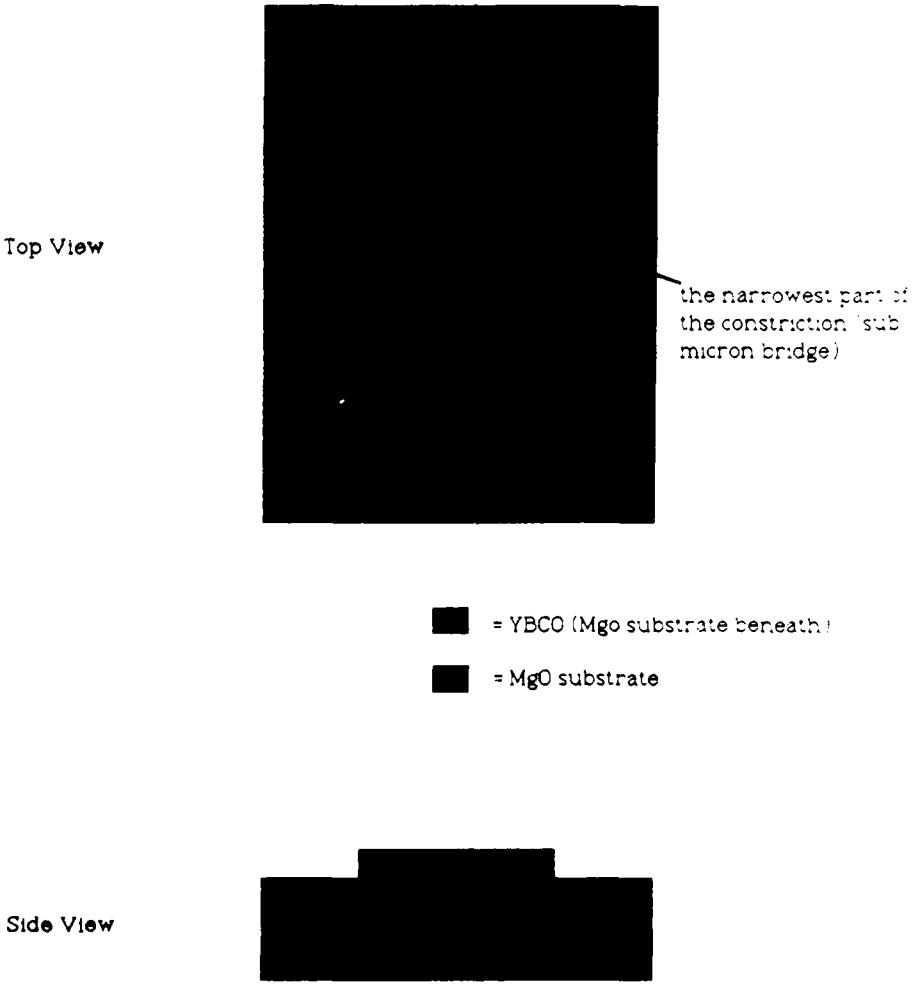


Figure 3a Schematic views of superconducting structure fabricated.

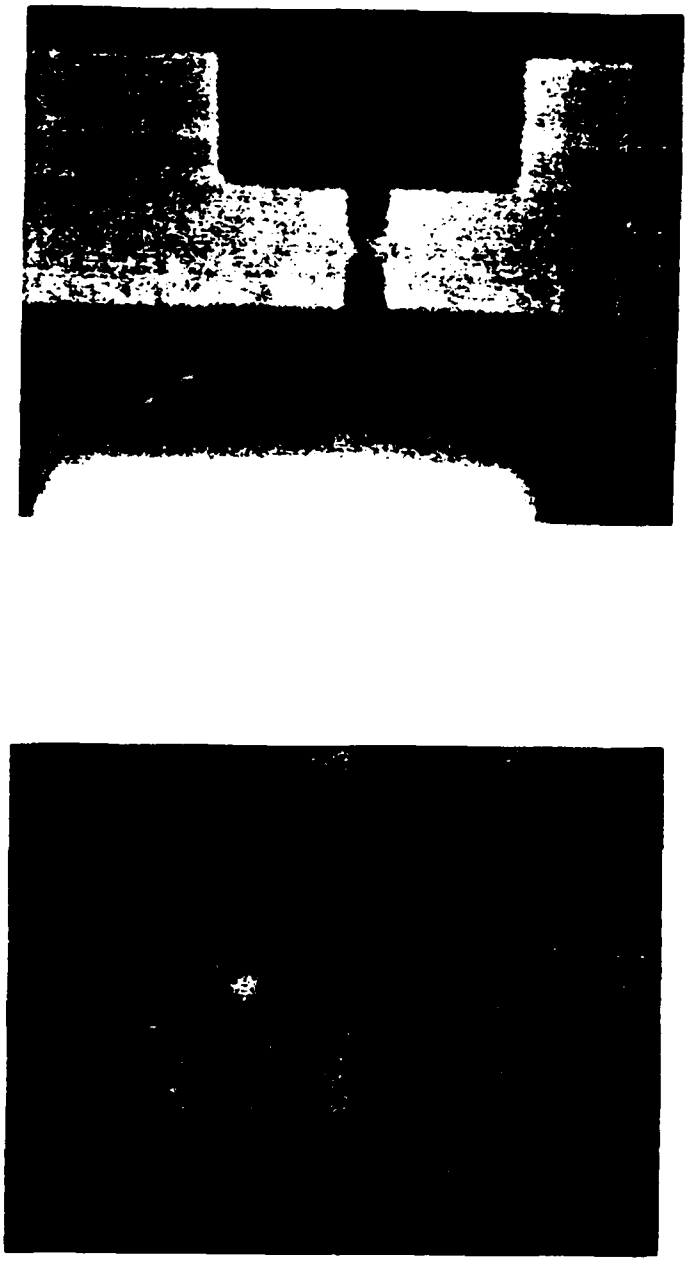


Figure 3b SEM view of one of the first structures fabricated.

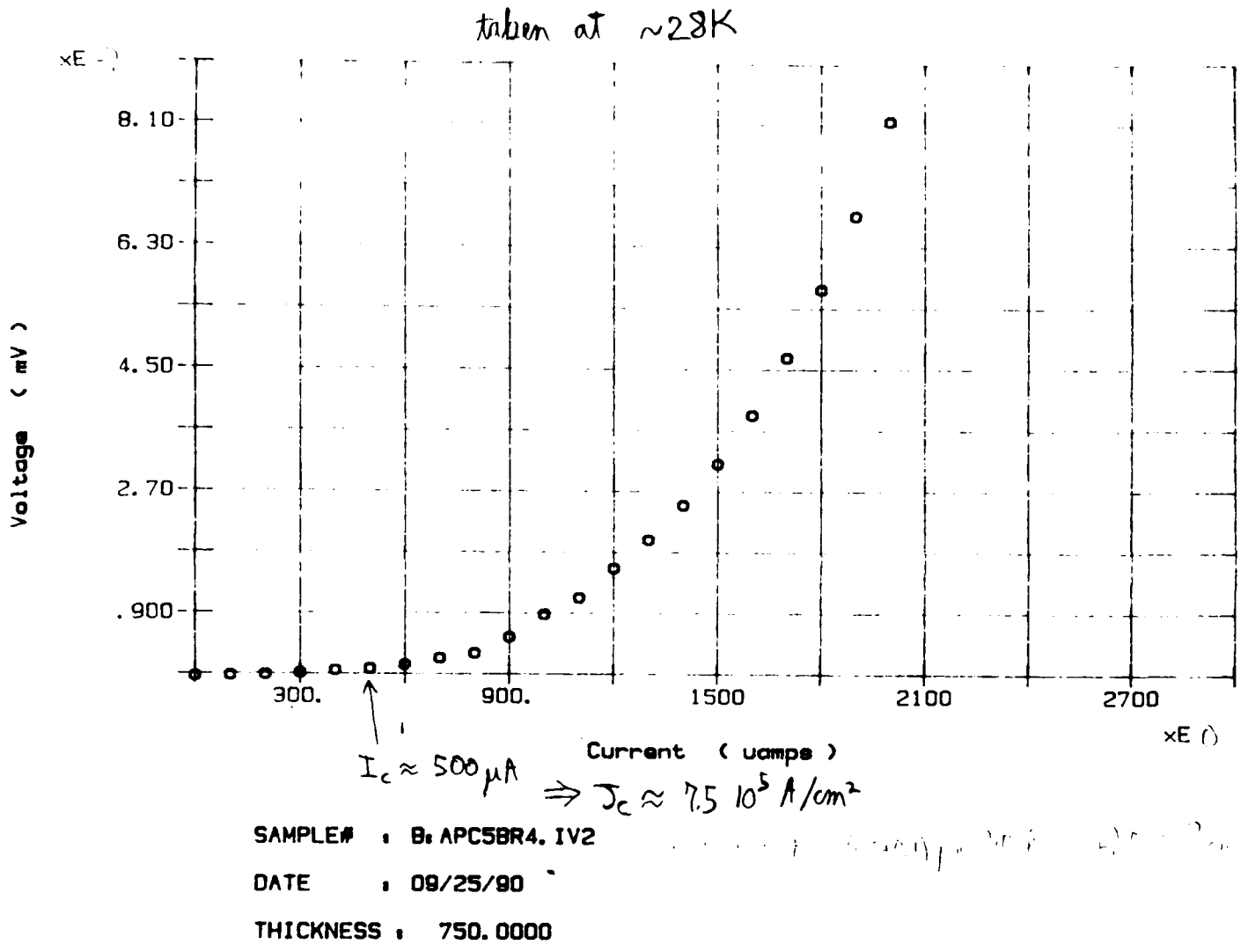


Figure 3c I/V characteristic curve of a representative junction structure.

JSEP Supported Publications

1. D. R. Allee, S. Y. Chou, J. S. Harris Jr. and R. F. W. Pease, "Engineering Lateral Quantum-Well Devices Using Electron Beam Lithography and Molecular Beam Epitaxy", *J. Vac. Sci. Tech.*, **B7** (6), Nov/Dec 1989.
2. S. Y.Chou, D. R. Allee, R. F. W. Pease and J. S. Harris, Jr., "Observation of Electron Resonant Tunneling in a Lateral Dual-Gate Resonant Tunneling Field-Effect Transistor," *Appl. Phys. Lett.* **55** (2), July 1989.
3. D. R. Allee, S. Y. Chou, J. S. Harris, Jr. and R. F. W. Pease, "Resonant Tunneling of 1-Dimensional Electrons Across an Array of 3-Dimensionally Confined Potential Wells", *Superlattices and Microstructures* **Vol. 7**, No. 2, 1990.

JSEP-Supported Dissertation

D. R. Allee "Nanometer Scale Device Engineering", Ph.D. dissertation, Stanford Electronics Laboratory, Stanford, CA, August 1989.

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[Allee] D. R. Allee, S. Y. Chou, J. S. Harris, Jr.and R. F. W. Pease, "Engineering Lateral Quantum-Well Devices Using Electron Beam Lithography and Molecular Beam Epitaxy", *J. Vac. Sci. Tech.*, **B7**, Nov/Dec 1989.

[Feuer] M. D. Feuer and D. E. Prober, "Step-edge Fabrication of Ultrasmall Josephson Microbridges", *Appl. Phys. Lett.*, **36**(3), 1 February 1980, pg. 226.

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[Schwartz] D. B. Schwartz, et al, "Microwave Power Spectra of Variable Thickness Sub-Micron Bridges", *IEEE Trans. Mag.*, **MAG-17** No.1, Jan 1981, pg.92.

Unit: 3

TITLE: Reactive Ion Profiling of Heterostructures

PRINCIPAL INVESTIGATOR: C. R. Helms

GRADUATE STUDENTS: M. Kniffin, G. Scott and T. Beerling

Scientific Objectives:

The objective of this work was to determine the surface chemistry associated with the interaction of reactive ions with GaAs and other III-V surfaces. Scientifically, this work represents an important new direction in studies of the interaction of neutral, stable molecules with surfaces. From a technological point of view, it will provide key information so that mechanisms of plasma and reactive ion processing of GaAs surfaces can be better understood. Our study will concentrate on the interaction of halogen containing molecular ions with GaAs surfaces. In-situ electron spectroscopy and mass spectroscopy techniques developed for similar studies of SiO2 and Si [Thomson 85], [Thomson 86], will be employed in this investigation. With this in mind, our specific objectives are:

1. To determine the relative importance of physical sputtering versus chemical reactions in GaAs reactive ion etching.
2. To determine the chemical nature of residues present during and after reaction ion bombardment.
3. Develop atomistic theoretical models to describe the combined effects of physical sputtering and chemical reactions during GaAs reactive ion bombardment.

Summary of Research:

In addition to the work proposed in this new contract, we have been continuing work begun on the previous program on metal-GaAs interfaces (the thesis work of Margaret Kniffin). This will be reported on first.

In our new work, since the program began, new results have appeared indicating the utility of low temperature deposition and etching in downstream plasma reactors (in both RF and ECR microwave configurations). With this in mind we are beginning construction of a UHV compatible downstream plasma source which will initially be used to investigate cleaning and etching of III-V surfaces and Device Structures.

Contacts to semiconductor devices are frequently subjected to elevated temperatures during post-deposition processing and subsequent device operation. Under these conditions many of the metals commonly used in the manufacture of GaAs devices will react with the underlying substrate. As contact properties are generally sensitive to interfacial chemistry, this can lead to significant variations in the electrical characteristics of a device over time. The extent of these interactions, the rate at which they occur and the effect that they have on diode behavior may ultimately determine the working lifetime of a device and thus must be fully characterized and understood.

Unfortunately, this information is often lacking or inadequate for even simple metal-gallium arsenide systems. In order to supplement the available literature, we have examined the interfacial reactions occurring at a number of different (Cr, Cu, Fe, Mn, Sc and Ti) metal-GaAs interfaces and attempted to correlate the variations in interfacial chemistry with the observed changes in contact properties. The intention was to obtain a broad overview of the effects of contact chemistry on metal-GaAs Schottky barrier heights, in the hopes of gaining some additional insight into the mechanisms which dominate Schottky barrier formation at these interfaces.

Interdiffusion and solid state reactions occurring at these interfaces were characterized, as a function of annealing temperature, using Auger sputter profiling. As expected, many of these metals (Cr, Cu, Mn and Ti) reacted extensively with the substrate upon annealing. The reaction kinetics generally seem to favor the formation of an arsenic-rich intermetallic phase at the original metal-semiconductor interface, as can be seen in from the Auger depth profile presented in Fig. 1. Sands and co-workers have made a similar observation for a number of other metal-GaAs systems, and suggested that this behavior was due to the relative immobility of arsenic at the early stages of the reaction [Sands].

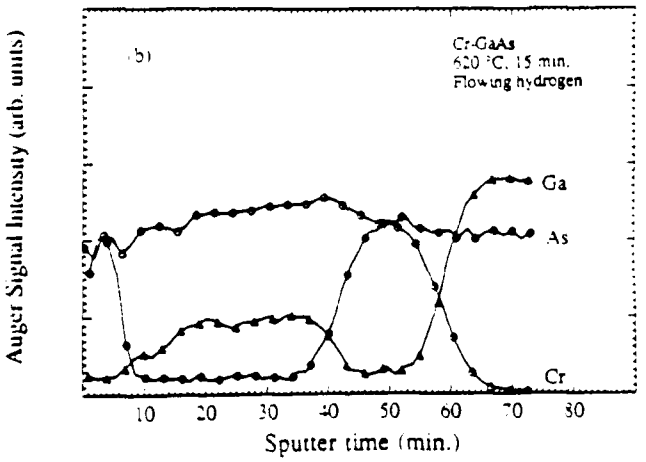

Figure 1 Auger depth profile of an annealed Cr-GaAs contact. The sample was annealed in flowing hydrogen for 15 minutes at 620° C.

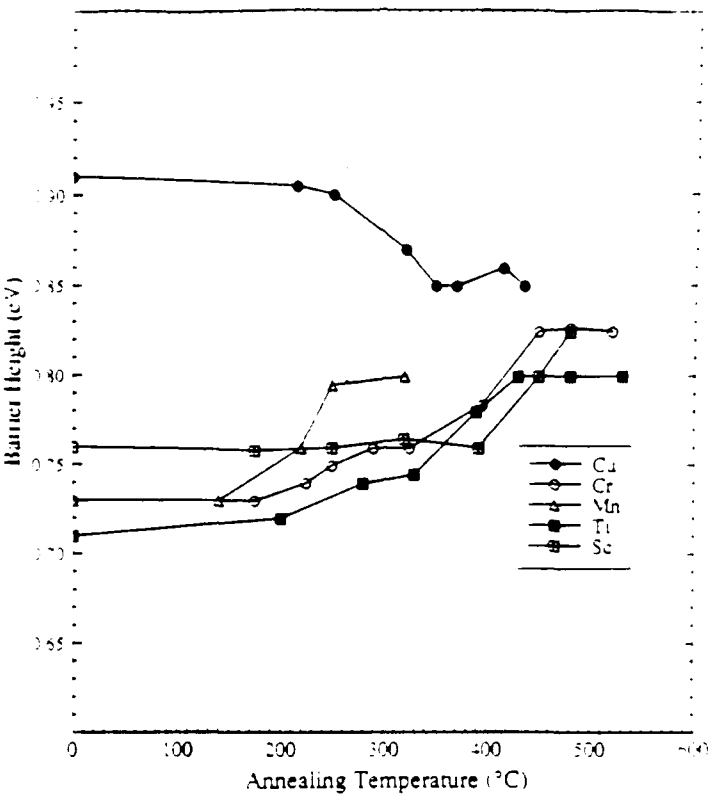

Figure 2 Variations in the n-type Schottky barrier height of Sc-, Ti-, Cr-, Mn- and Cu-GaAs contacts as a function of annealing temperature. Barrier heights were determined from current-voltage measurements.

The corresponding changes in the n-type metal-GaAs Schottky barrier heights were monitored using a combination of current-voltage, capacitance-voltage and photoresponse measurements. The results are summarized in Fig. 2, in which the n-type Schottky barrier heights are plotted as a function of annealing temperature. The plotted barrier heights are the values extracted from current-voltage measurements, however similar results were obtained using other methods of barrier height determination.

An abrupt change in the metal-GaAs Schottky barrier height is generally observed upon annealing. One can see that this results in a significant reduction in the range of measured barrier heights, with the barrier heights for all of the annealed contacts falling somewhere between 0.80 to 0.85 eV regardless of the as-deposited barrier height.

For the Ti-, Cr-, Cu- and Mn-GaAs interfaces, the change in the Schottky barrier height that occurs after annealing could be associated with the appearance of a metal arsenide (or arsenic-rich intermetallic) phase at the original metal-gallium arsenide interface. Furthermore, we found that once a uniform arsenide layer was formed at the contact interface, the n-type barrier heights tended to stabilize between 0.80 to 0.85 eV. Analogous behavior has been reported in both the Al-GaAs [Newman], [Johnson] and Rh-GaAs [Yu] systems as well. The similarity between the electrical and chemical properties of these systems suggests that there is a link between barrier height and interfacial chemistry.

Downstream Plasma Processing

Recent work using downstream plasma processing for low temperature depositions have resulted in operating MIS devices on GaAs [Fountain] as well as high quality Si MOS devices [Richard] using low temperature grown oxides. These existing results have led us to change direction for the future in this program to construct such a reactor on an existing UHV surface analysis system. In our first experiments with this approach the utility of such a reactor, operating with either hydrogen or oxygen, for surface cleaning will be assessed. Other plans include the investigation of Si-Ge deposition and SiO_2 deposition on both Si and GaAs at low temperatures for surface passivation.

To perform these studies, a variety of in situ spectroscopic tools will be employed in a UHV analysis system. This study will focus on the following subjects; cleaning of Si and GaAs surfaces using hydrogen plasmas, passivation of GaAs surfaces, plasma enhanced epitaxial growth of Si and Ge, and plasma enhanced deposition of SiO2 and Si_3N_4 on Si and GaAs.

Experimental

Shown in Fig. 3 is a diagram of the UHV system to be used in this study. Plasmas can be generated upstream from the samples either by an inductive coil, operating at 13.56 MHz, or by an Electron Cyclotron Resonance Source (ECR), operating at 2.45 GHz. At this present time, the system is equipped with an inductive coil. Since the pressures necessary to sustain plasmas are generally much higher than the maximum allowable pressures when operating many spectroscopic tools, a differential pumping stage, pumped on by a turbomolecular pump, is used to reduce pressures in the main chamber to the allowed values. Pressures in the differential pumping stage and chamber are sufficiently low enough so that excited species do not relax before reaching the samples.

In the chamber, a quadrapole mass spectrometer (QMS) is positioned line-of-site with the plasma so the excited species in the gas phase may be analyzed. With the heater

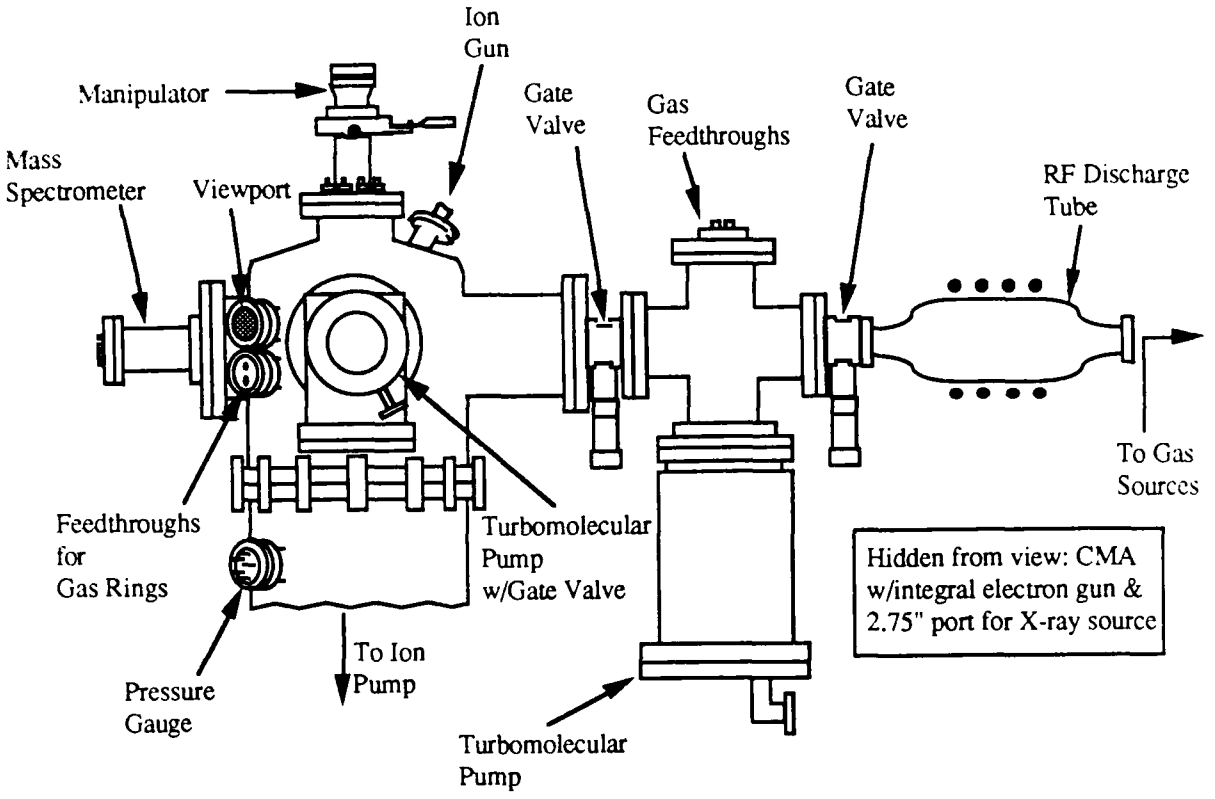

Figure 3 UHV system to be used in study.

assembly on the sample tray, the QMS can also be used to perform Temperature Programmed Desorption studies (TPD). To analyze the samples, Auger Electron Spectroscopy (AES) or X-Ray Photoemission Spectroscopy (XPS) may be performed. The chamber is presently equipped with an AES system, although a double pass CMA and X-ray source are readily available.

Surface Passivation of GaAs

Studies of surface passivation of GaAs surfaces, using hydrogen plasmas, have been performed. [Gottscho] et al have shown increases in GaAs photoluminescence (PL) intensities during exposure to a hydrogen plasma. This increase in PL intensity implies a reduction in surface recombination velocity, which in turns suggests a reduction in the interface state density. Atomic hydrogen, supplied by the plasma, is removing excess As (in the form of AsH_3) from the the GaAs surface [Capasso]. This excess As at the GaAs surface is believed to be the cause for fermi level pinning at the GaAs surface [Callegari]. GaAs MOS structures have been built [Callegari] where GaAs surfaces are first exposed to

a hydrogen plasma to reduce the As surface concentration and then exposed to a nitrogen plasma to grow a thin nitride layer. Gallium oxide was then deposited on the nitride layer. Interface state densities for these structures are believed to be about 10^{11} eV-1 cm^{-2} (an exact value could not be determined as the oxide was very leaky).

In our work, we wish to further pursue the subject of GaAs surface passivation. Work is to be performed where, along with hydrogen and nitrogen plasma treatments, other gases, such as ammonia (NH3), will be used. XPS will be used to determine the chemical effects of such a treatment. Structures to further examine the effects of the plasma treatment will be constructed. Metals of differing work functions will be deposited onto GaAs samples that have gone through a processing sequence which both removes excess arsenic and creates an ultrathin nitride layer, thin enough to permit tunneling. Barrier heights will be determined to see if the fermi level has been unpinned. MOS structures will be fabricated, but with oxides superior to the gallium oxide used in the work of [Callegari] so that a more reliable value for interface state densities may be determined.

Remote Plasma Enhanced Chemical Vapor Deposition (RPECVD)

Work has been performed using RPECVD [Lucovsky] resulting in low temperature epitaxy of Si [Breaux], Ge [Rudder], and deposition of high quality SiO_2 [Fountain] and Si_3N_4 [Tsu]. Our goal is to continue these studies by; improving plasma cleaning procedures to prepare substrates for RPECVD, improving thin films grown by RPECVD, epitaxially growing Si and Ge and depositing SiO2 and Si_3N_4 using processing gases that have not yet been rigorously examined, and depositing SiO_2 on GaAs for passivation purposes (as described earlier).

ECR sources have been used for some time for etching and deposition of dielectrics. Although there are many studies which have examined the character of ECR sources, research in this area has yet to be exhausted by any means. Work will be done where we replace our inductive plasma system with that of an ECR. This will give us the opportunity to study how changes in ECR source parameters, such as input power, reflected power, and magnetic field profile and strength effect the density and type of excited species generated by the ECR plasma. RPECVD studies will also be performed using the ECR source as the source for excited chemical species.

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1. M. Kniffin and C. R. Helms "The Synthesis and Properties of Low Barrier Ag-Ga Intermetallic Contacts to n-type GaAs" *J. Appl. Phys.* **68**, 1367 (1990).

2. E. Weiss, R. C. Keller, M. Kniffin and C. R. Helms, "Selective Oxidation and Etching of Reacted Pt Films on GaAs", *Mat. Res. Soc. Symp. Proc.* **181**, 253 (1990).

JSEP Supported Presentations

E. Weiss, R. C. Keller, M. Kniffin, C. R. Helms "Selective Oxidation of Reacted Pt Films on GaAs", 1990 Spring Meeting of the MRS, San Francisco.

Unit : 4

TITLE: GaAs on Si Integrated Circuits

PRINCIPAL INVESTIGATOR: B. A. Wooley

GRADUATE STUDENT: G. Nasserbakht

Scientific Objective:

The objective of this research is to explore means by which newly emerging compound semiconductor technology, such as heteroepitaxial GaAs on silicon, can be exploited at the circuit and system level. The emphasis of the program is on the application of GaAs/Si technology to optoelectronic circuits for broadband communications.

Summary of Research:

The principal focus of this research has been on the design and integration of fiber-optic receiver front ends in GaAs/Si technology. In fiber-optic communication systems, stringent bandwidth and sensitivity requirements are placed on the receiver electronics. These requirements are especially significant at the front end of the receiver, where optical information is converted to an electronic format and subsequently amplified by a preamplifier. Monolithic integration of the photodetector and the preamplifier offers a significant improvement in performance by reducing the parasitics associated with the interconnection between these components.

An objective of this research has been the fabrication of a GaAs photodetecting diode on a silicon substrate in which a receiver front end has been integrated. During the past reporting period, we described a functional, fully integrated GaAs/Si receiver front end, which consisted of a GaAs metal-semiconductor-metal (MSM) photodetector and a Si bipolar preamplifier. This was the first reported integration of GaAs components and Si bipolar circuits. Recently, considerable effort has been devoted to improving the process flow for the integration of the GaAs and Si devices, with the objective of simplifying the integration of the back-end processing steps that follow the fabrication of the Si devices and GaAs epitaxial growth. These modifications have resulted in a new generation of the process flow.

One major obstacle that has presented itself in all fabrication runs since the beginning of this research, has been the metal etch process. In order to provide adequate metal coverage of the dielectric steps near the photodiode edges, a fairly thick (1μm) metal layer was used.

The use of a wet chemical etch was therefore not feasible because of the small contact size and spacing regions in the Si device areas. A chlorine-based plasma etch process etch system was therefore adopted. The Al etch results on the partial wafers used in this project were quite nonuniform, with substantial undercutting of the metal lines. It was extremely difficult to achieve an acceptable metal etch even after reoptimizing the system for the partial wafer conditions. The problem was initially attributed to poor thermal contact between the holder that is used to carry the partial wafer through the system and the chuck in the etch chamber. Results from recent etch tests, however, have revealed a phenomenon that traces the problem to the metal mask.

The chemical reaction in the metal etch chamber is an exothermic reaction. During the etch, the wafer temperature increases due to particle bombardment from the plasma as well as the heat released from the reaction during the etch. Metal masks used for VLSI circuits usually protect a fairly large area of the wafer from the etch. Masks that are made for special purposes, however, do not always follow this convention. If the area of exposed metal is large enough, the amount of heat generated by the reaction can no longer be easily dissipated away from the wafer. This results in the heating of the wafer, which can severely degrade the photoresist.

The circuits for this project were fabricated in a small area of a much larger design. Since prior to the generation of the metal mask, the data for the metal lines for the rest of the wafer were removed to protect proprietary information, a large area of the wafer was exposed to the metal etch. To rectify the problem, a new metal mask is being generated that exposes a much smaller area of the metal to the plasma etch and should significantly improve the etch results.

In order to investigate the effects of GaAs MBE growth and subsequent processing steps on Si MOS devices, several wafers with various device structures have been fabricated in a 1μm CMOS process at Intel Corporation. These wafers are currently going through the back-end processing steps and will provide useful information on the effects of monolithically integrating GaAs and Si devices on MOS device performance.
As another part of this research, we have been investigating the design of the front end receiver in CMOS technology and its integration with a GaAs MSM photodiode. The main objective of this research is to achieve a low-noise, wide-bandwidth receiver in a technology (Si CMOS) that affords significantly higher levels of integration for the complete receiver. For example, the timing and data recovery circuits that follow the preamplifier might be included with the receiver front end on a single chip. An important issue in the design of such a receiver is the input stage, since it limits the sensitivity of the receiver.

Several different preamplifier input configurations, common-source, common-gate, and source-follower, have been investigated. Although the noise contributions of the active device in the various configurations can be very similar, the input referred noise contributions of the stages following the input stage are different due to the different transfer gains. Results of the analysis suggest that a common-source configuration is best suited for low noise operation. To optimize the noise performance, the size of the input stage is chosen such that the input capacitance of the amplifier is equal to the sum of the photodiode capacitance and the parasitic interconnection capacitance between the photodiode and the preamplifier. Since the noise minimum is fairly broad, the actual size of the input device is chosen to be smaller than the optimum value. This reduces the area and power dissipation, while maintaining the noise level close to the minimum value.

Unit: 5

TITLE: THE ELECTRONIC STRUCTURE AND INTERFACIAL PROPERTIES OF HIGH TEMPERATURE SUPERCONDUCTORS

SENIOR PRINCIPAL INVESTIGATOR: W. E. Spicer

POST DOCTORAL FELLOW: Z. X. Shen

GRADUATE STUDENTS: B. O. Wells, D. S. Dessau, D. King and E. R. Ratner

Scientific Objectives:

The Cu-O based high temperature superconductors have been extensively studied since their discovery in 1986. While many advances have been made in our understanding of these unique materials, fundamental questions remain concerning the underlying physics of these materials and their technological applications. Our research has aimed at developing a thorough understanding of the electronic structure of these the superconductors as well as studying interfaces of the superconductors with metals for both basic physics and technological concerns.

Summary of Research:

We have used a variety of surface science techniques to study high temperature superconductors. Our emphasis is on photoemission spectroscopy which gives detailed yet simple to interpret information on the occupied density of electronic states. In particular we are now beginning to work with very high resolution, angle resolved photoemission with energy resolution as good as 18 meV. This is an order of magnitude better resolution than was available in photoemission only a few years ago and allows studies of small features such as the superconducting energy gap.

A. The Au/Superconductor Interface

In last year's report we detailed the preliminary work we had performed studying the metal/superconductor interface. Continuing experiments have been very productive, in particular studying the interface of Au with the high temperature superconductors.

Last year's work established that a Au overlayer caused little to no change in the position and shape of the core electron energy levels of the $Bi_2Sr_2CaCu_2O_{8+\delta}$ superconductor [Wells '89]. This indicates that there is very little if any chemical reaction

between Au and $Bi_2Sr_2CaCu_2O_{8+\delta}$. To further investigate the Au/superconductor interface we tested whether the Au overlayer affected the electrons in the valence band near the Fermi level. Since the electrons nearest the Fermi level are responsible for conductivity, changes in these states are the most important for the physical properties. The experiment we performed used photoemission at normal emission with a relatively large photon energy (75 eV) and an overall energy resolution of 200 meV. A very small overlayer of Au, such as the 1/2 Å used in this experiment, is not metallic and therefore does not have states at the Fermi level and thus does not complicate the signal from the superconductor in this energy region. We found that for the Au/$Bi_2Sr_2CaCu_2O_{8+\delta}$ interface there were no detectable changes in the near Fermi edge states. For the Au/$YBa_2Cu_3O_7$ interface there was a decrease in the number of states at the Fermi level indicating that the interface formation caused a disruption of the metallicity of the surface of the $YBa_2Cu_3O_7$ material.

Additional more insightful experiments were performed on this materials system. Some background is necessary is necessary to understand the results. A traditional superconductor in good electrical contact with a normal metal will induce superconductivity in the metal over a distance of several microns - this is known as the proximity effect. With the advent of new very high resolution photoemission techniques, it has been shown that it is possible to detect the effects of the superconducting gap with photoemission [Olson]. This has raised the possibility that we could detect a proximity effect gap in a metal overlayer on the high T_c superconductors. There are two interfaces that we feel would be particularly advantageous for detecting the proximity effect. The inert nature of the Au/$Bi_2Sr_2CaCu_2O_{8+\delta}$ single crystal interface mentioned above, naturally suggests that this system would be a good candidate for observing the proximity effect. Another good possibility for observing the proximity effect is in the Au/$YBa_2Cu_3O_7$ a axis thin film since the coherence length of the superconducting pairs is much longer along the a axis than the c axis. (Single crystals cleave with the c axis normal to the surface and that is how most films grow.) This second interface is difficult to study since thin films of $YBa_2Cu_3O_7$ cannot yet be adequately cleaned for photoemission. We devised a system where we deposited the Au overlayer immediately after growing the film to preserve the good interface and then cleaned the Au surface for photoemission by sputtering. Our experiments that searched for a proximity effect gap were performed with a resolution of 30 meV. We were not able to detect a superconducting gap in the Au overlayers in either case. We were able to put an upper limit on the size of any proximity gap of 5 meV for the particular interfaces studied here. This has strong implications for methods for fabricating Josephson junctions or any application that depends on surface superconductivity.

While the investigation of the Au/$Bi_2Sr_2CaCu_2O_{8+\delta}$ single crystal interface with

ultrahigh resolution did not reveal evidence of a proximity effect, it did provide an unexpected insight into the nature of the $Bi_2Sr_2CaCu_2O_{8+\delta}$ material itself. As mentioned above, low coverages of Au allow us to detect electronic state changes in the superconducting substrate near the Fermi level. When we measured the 1/2 Å Au/$Bi_2Sr_2CaCu_2O_{8+\delta}$ single crystal interface with 30 meV resolution, angle resolved photoemission, we found changes not previously detected. Along the Brillouin zone edge the Au caused no change to either the states at the Fermi level in the normal state or to the gap structure in the superconducting state. However, along the Brillouin zone diagonal both of these features were destroyed when the Au overlayer was deposited. The material consists of cation-oxygen layers. Only two layers in this material can possibly contribute electronic states at the Fermi level: the Bi-O layer and the Cu-O layer. Earlier experiments have shown that the Bi-O layer forms the cleavage plane while the first Cu-O layer is about 5 Å deep [Lindberg]. Since it is highly unlikely that a Au surface layer could disrupt a deeper layer (Cu-O) without disrupting the surface layer (Bi-O) we can conclude that the region which was disrupted (the zone diagonal) had strong Bi-O character while the region undisturbed (the zone edge) is of almost purely Cu-O character. These are the atomic characters predicted by band theory. This work was published after the time period of this report but for convenience is included as a reference [Wells '90]. Another conclusion that can be drawn from this experiment is that for the undisturbed material the superconducting gap exists undiminished up to the atomic surface. This is contrary to predictions made based on conventional 3-d Ginzburg-Landau theory and has strong implications for theories of the mechanism of high temperature superconductivity.

B. Electronic Structure of Various Superconductors

We have performed several studies on the electronic structure of different families of superconductors. One experiment we performed determined the symmetries of states in different energy regions of the valence band in $Bi_2(SrCaLa)_3Cu_2O_8$. Selection rules allow only states of certain symmetries to be excited by radiation of given polarization and orientation. Since light from a synchrotron is highly polarized, we were able to vary the angle of the electric field vector with respect to the sample and thus vary the symmetry of the states that dominate the photoemission spectrum. A comparison of spectra showed that the states near the Fermi level were of D5 symmetry (O $2p_x$ and $2p_y$) while states at the highest valence band binding energies were of D1 symmetry (O $2p_z$). This result limits the symmetry of states that can be involved in the pairing process since it is the electrons near the Fermi energy that are paired in the superconducting state, and thus the implication for theory is obvious.

We have also studied the electronic structure of $Pb_2Sr_2PrCu_3O_8$. We note that for the family of compounds $Pb_2Sr_2LCu_3O_8$ that for L = any rare earth element the material is superconducting. However, the family of compounds $RBa_2Cu_3O_7$ is superconducting for

R = any rare earth except Pr, when the compound is insulating. We find that the main difference in the electronic structure of the two compounds with Pr is that the hybridization between the Pr 4f states and the Cu-O valence band states is greatly reduced in the superconducting $Pb_2Sr_2PrCu_3O_8$ compound compared to the insulating $PrBa_2Cu_3O_7$ material. This is physically reasonable because there is a larger real space separation between the Pr ions and Cu-O layers in the superconducting compound. This data, along with earlier data on the $RBa_2Cu_3O_7$ materials [Kang] suggests that the critical factor for quenching superconductivity is the amount of hybridization to, or disruption of, the Cu-O states.

The next stage of our research on high temperature superconductors is focussing on the detailed information that can be gained about the superconducting state by examining the superconducting gap with ultra-high resolution photoemission spectroscopy. In addition to providing a fairly simple measure of the spectral weight function of the material in the superconducting state, photoemission can provide k resolved information about the superconducting gap that has not been available before from any experimental technique.

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Unit: 6

TITLE: Semiconductor Laser Structures for Optical Interconnects

PRINCIPAL INVESTIGATOR: S. S. Wong

GRADUATE STUDENT: S. Biellak and W. Cheng

Scientific Objectives:

The objective of this work is to study the interplay between geometry and physics in a semiconductor laser in order to achieve ultra-low threshold current and high efficiency for applications in inter-chip optical data communication.

Summary of Research:

As integrated systems become increasingly complex, a limiting factor in the performance is the rate at which data can be communicated onto and off of the integrated circuit chip. Optical links can potentially deliver the high data rate required. Future systems may contain tens or hundreds of semiconductor lasers monolithically integrated onto a substrate. The threshold current and the quantum efficiency of the lasers will play a key role in determining the power dissipation, reliability and overall efficiency of the system.

1. Dry Etching Technique for Semiconductor Lasers

Semiconductor lasers with quantum wells, which provide one-dimensional confinement of carriers, have proven to be extremely efficient devices. Theoretical calculations have shown that two-dimensional confinement using a quantum wire structure will further reduce the threshold current and improve the efficiency [Yariv]. One method to create the quantum wire is using a highly anisotropic dry etching technique. One such technique has been developed for etching the laser facets [Behfar-Rad a]. Through the combination of contrast enhanced lithography, a silicon dioxide mask and chemically assisted ion beam etching, very vertical and smooth facets have been achieved. GaAs/AlGaAs lasers with the etched facets exhibit no degradation in the threshold currents when compared to devices with cleaved facets [Behfar-Rad b]. The dry etching technique is independent of crystal orientation, and hence has been used to form lasers with a V-shaped cavity. These devices show that total internal reflection (with minimal loss) can be achieved at a bend [Behfar Rad c]. The etching technique has been employed to define the ridges and the facets in a four-mask process for the fabrication of monolithic ridge lasers [Behfar-Rad d]. Using this process and extending the concept of the V-shaped cavity, ridge lasers with a

triangular shaped cavity have been demonstrated. A scanning electron microscope photograph of the triangular ridge laser is shown in Fig. 1. In this unconventional laser, two of the three facets are positioned such that the incident angle is larger than the critical angle, which results in total internal reflection. The third facet has an incident angle just below the critical angle, and hence is partially transmissive. The reflectivity at the light emitting third facet can be adjusted by changing the incident angle and is higher than that of a conventional facet. Consequently, the triangular laser exhibits a threshold current lower than that of a rectangular device with a similar cavity length. When the ridge is wider than 3μm, the laser is bi-directional. When the ridge is narrower than 3μm, however, the laser becomes uni-directional as illustrated in the far field patterns of Fig. 2. Theoretical calculations of the lateral modal pattern confirms that the laser has only one allowed lateral mode for a ridge narrower than 3μm. One aspect seen in the far-field patterns is that the left-hand lobe is always more intense than the right-hand one. This non-reciprocal behavior is geometrically controlled and probably arises from fabrication asymmetries such as a difference in the incidence angles of the two legs of the triangular ridge laser to the output facet. The spectra of a triangular ridge laser is shown in Fig. 3. At threshold, the laser exhibits multi-longitudinal-mode behavior. Above threshold, however, the device becomes single longitudinal-mode, which is a characteristic of the travelling wave laser.

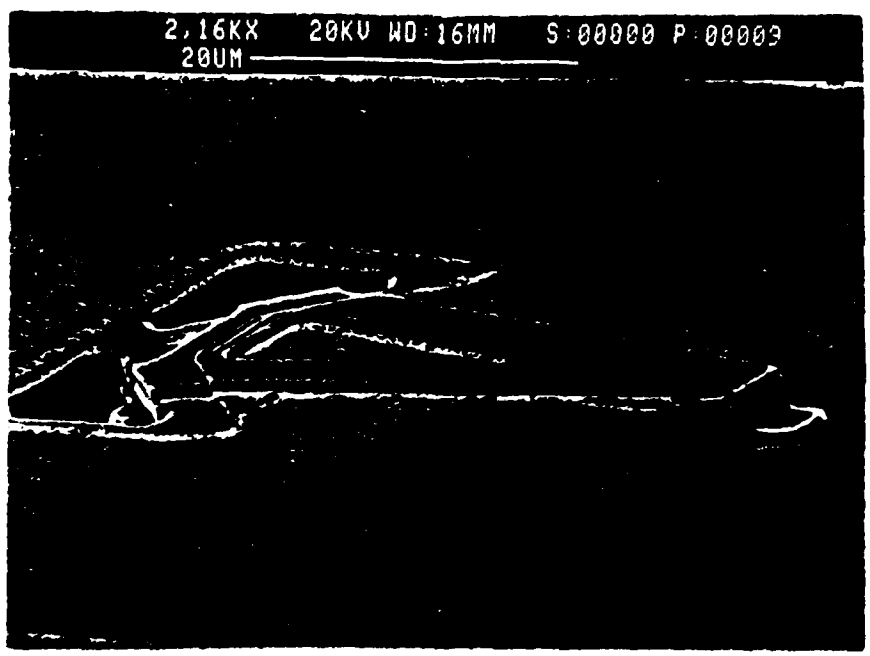
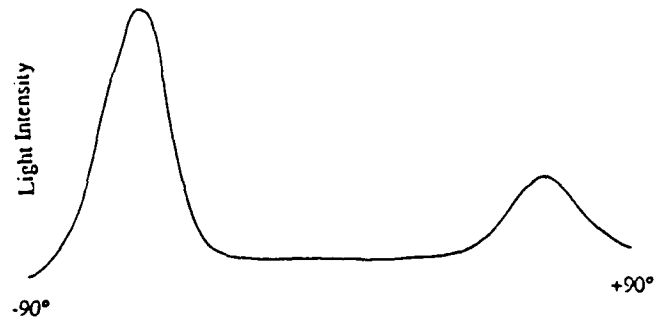


Figure 1 SEM photograph of a triangular ridge laser.

(a)



(b)

Figure 2 Far field patterns for triangular ridge lasers with a (a) 3.5 μm, and (b) 2.5 μm wide ridge.

(a)

(b)

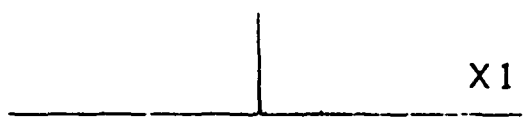


Figure 3 Spectra characteristics of a triangular ridge laser (a) at, and (b) above threshold.

2. Nanometer Lithography

In order to observe quantum wire effect, lateral dimension has to be on the order of 100 nm. Electron beam direct write lithography is required to pattern such fine features. Figure 4 shows 200 nm wide lines and 300 nm wide spaces defined by the electron beam lithography and a negative resist. Although the profile is less than ideal and the edges are rough, we believe that the technique can be fine tuned.

Figure 4 - SEM photograph of 200 nm wide lines and 300 nm wide spaces.

Future Direction

With further development of the electron beam lithography and the dry etching technique, quantum wire structures will be fabricated and evaluated with photoluminescence technique. It is anticipated that by comparing the luminescence behavior of the various wire structures and the control sample, the damage from the dry etching can be assessed and its applicability to fabricating quantum wires can be determined.

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2. A. Behfar-Rad, S. Wong and J. Ballantyne, "Travelling wave operation in a triangular-shaped monolithic semiconductor ring laser," International Electron Devices Meeting, December 1990.

UNIT: 7

TITLE: Quantum Computing

PRINCIPLE INVESTIGATOR: J. D. Plummer

GRADUATE STUDENT: B. Biegel

Scientific Objectives:

The objectives of this research are three-fold. First, we hope to contribute to the understanding of ways in which quantum effects can be used to facilitate the operation of electronic devices which are potentially much more efficient and highly integrable than conventional electronic devices. Second, and central to this research, we will develop a numerical simulation tool for the simulation of these quantum electronic devices. Finally, we will test this simulator's predictions by fabricating and testing our own SiGe-based quantum devices and by comparing its predictions with other researchers' results for GaAs-based quantum device operation.

1. Motivation and Significance

Tremendous advances have been seen in digital electronics technology in the past three decades due to a strong market demand for greater system functionality. However, in an effort to improve the speed and functionality of integrated circuits (ICs), decreasing device dimensions are becoming comparable to the quantum wavelength of the charge carriers used in device operation. As devices continue to shrink towards this quantum realm, conventional transport (based on drift and diffusion of carriers) will be besieged by "parasitic" quantum effects caused by the wave nature of carriers [Ferry]. These include such effects as oxide tunneling in MOSFETs and quantum reflections in HBTs. This increasing encroachment of quantum effects into conventional device operation is by itself sufficient motivation for the research of quantum phenomena in electronic systems. Through publications from this work, we hope to convince a greater circle of electronics researchers of the importance of understanding quantum effects, even if one's interest lies only in conventional electronic systems.

There is another potentially more important motivation for the study of quantum phenomena in electronic systems. This is the possibility of using quantum effects as controlling mechanisms, rather than suppressing them, in the operation of electronic devices [Bate1]. The science of using quantum mechanics to produce some form of computation will be called quantum computing. The potential advantages of quantum

computing over conventional electronics technology are clear. First, embracing quantum phenomena for electronic device control would allow (in fact require) at least one device dimension to be scaled into the quantum realm, rather than requiring all dimensions to be much larger than quantum-scale. Thus, quantum-scale integration of electronic devices would make possible orders of magnitude higher integration densities than conventional VLSI or even ULSI. Second, as we know from conventional electronics, the smaller the devices, the faster their potential operation. Thus, quantum-scale systems have a much higher processing speed potential. Third, using quantum effects in the operation of electronic devices would allow us to use to our advantage all of the phenomena that are parasitic in conventional devices, and presents the possibility of much higher switching efficiency.

Given the above motivation, how can we most efficiently build an understanding of quantum computing. Because of the increasing cost of conducting experimental research as electronic devices shrink, an increasing amount of state-of-the-art electronics research is being conducted through more precise theoretical analyses and numerical simulations. The cost of experimental trial-and-error is even more expensive with quantum-scale integration, and in some cases, the needed technology does not even exist yet. Faced with these limitations, this research concentrates on the development of a theoretical and simulation foundation for quantum computing. Our theoretical investigation of quantum computing addresses the more general issues, such as what characteristics a quantum computing system will have, and what characteristics quantum computing itself will have. On the other hand, our efforts to develop a quantum simulation capability answers the need to examine in detail particular quantum phenomena and devices, to determine accurately how quantum systems will operate and thus whether we can extract useful computing from them. To test the accuracy of our simulation tool, we will fabricate simple quantum effect devices in the SiGe material system. We will also compare its predictions for GaAs-based structures with experimental data from other researchers.

2. Progress

The basic direction of knowledge flow in this research project is from the more general to the more specific: from theory to simulation to experiment. Our theoretical investigations of quantum computing serve to guide our simulation efforts, which in turn will guide our experimental efforts. Thus, we will present the results of our work in this order. Because the central objective of this work is the development of an accurate quantum device simulator, more space will be given in this report to progress made towards this objective.

Some of the results of our theoretical investigation of quantum computing are evident in the motivation for this research, as discussed in the previous section. These are that

quantum computing systems have the potential for much higher integration density, higher speed, and lower power than conventional (drift-diffusion) electronics. The realization of this potential will not be easy, due to the fact that quantum computing proposes to use completely different phenomena to control the operation of electronic devices. Our ability to make quantum computing a reality may well depend on our ability to look at computing in a new way: with our present knowledge, but without our usual preconceptions. Our theoretical investigation is based on this philosophy.

In spite of the revolutionary nature of quantum computing, its development is greatly aided if we recognize and use two excellent sources of knowledge: conventional electronics and optical processing systems. The dual nature (wave and particle) of charge carriers creates a dual nature of quantum effect circuits, allowing us to use concepts and insight from both (particle-based) conventional electronics and (wave-based) optics. On one hand, charge carriers in the quantum circuit propagate according to wave mechanics, as in optical systems, while at the terminals of the quantum circuit, our input and output signals are voltages and currents, as in conventional electronics. It is a direct result of the advancement of conventional electronics that quantum computing has become possible, but it is also because of this advancement that quantum computing has become (almost) needed. In conventional electronics, the attitude towards quantum phenomena is to ignore, suppress, or overwhelm them, and thus maintain reliable device operation based on classical phenomena. The challenge of quantum computing is to reverse the conventional approach: to make the wave nature of carriers dominant and to use it to overcome limitations faced by conventional electronics.

There is a strong analogy between optical processing systems and quantum computing systems, since both are wave processing systems. Since optical processing is much more advanced than quantum computing, we can use this "optical analogy" very effectively in the development of the science of quantum computing. For example, we can identify functionally similar device components in quantum computing systems and optical processing systems (e.g., waveguides, reflectors, and resonant cavities) [Randall]. The structure and nature of computing will likely be similar in the two systems as well. Rather than a two dimensional array of selectively interconnected and independent simple switches as in conventional electronics, a quantum computing circuit will more likely be a three dimensional integrated circuit of limited interconnect nodes with high functionality. Computation will be realized in a distributed and massively parallel manner (holographic computing) [Bate 88] [Reed] [Capasso 89]. Given this concept of quantum computing, it may turn out that quantum integrated circuits will not be well suited to digital computation, but they may be perfectly suited to artificial intelligence type decision making.

We now discuss the results of efforts to develop a general quantum device simulator. Our quantum simulation tool is based on the Wigner function formulation of quantum mechanics [Mahan 90], because the quantum transport equation (QTE) for the Wigner function (WF) is the quantum mechanical analog of the Boltzmann transport equation [Mahan 87], which is used to simulate classical electronic systems. The Wigner function formulation has been used by other researchers to simulate quantum electronic systems [Frensley] [Jensen 1]. By the WF method, a quantum system is simulated by solving the QTE for the Wigner function. We chose the resonant tunneling diode (RTD) as the standard device structure to be modeled in our simulations for several reasons: 1) the RTD is the simplest structure in which the basic quantum phenomena, quantum coupling and quantum confinement, are important; 2) the RTD is highly studied and well understood [Capasso 86], allowing us to assess the validity of our simulation results; and 3) the RTD has a very fast response [Sollner], allowing us to test the capabilities of our simulator to accurately model very fast quantum systems. All simulation results given in this report are for a p-type SiGe RTD, the structure and (biased) energy band diagram of which are shown in Fig. 1.

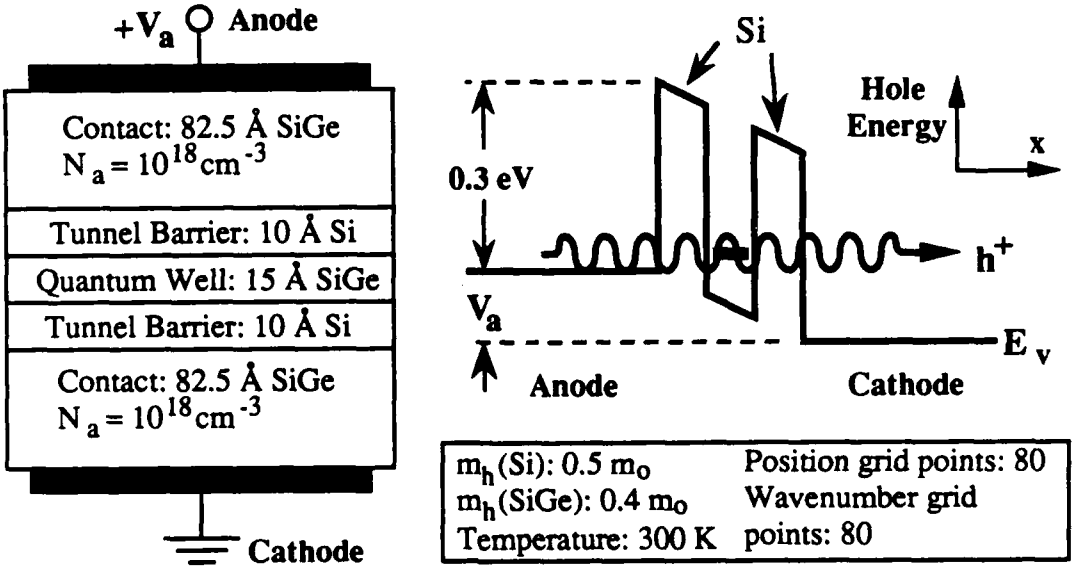

Figure 1 SiGe RTD structure, energy band profile, and simulation parameters.

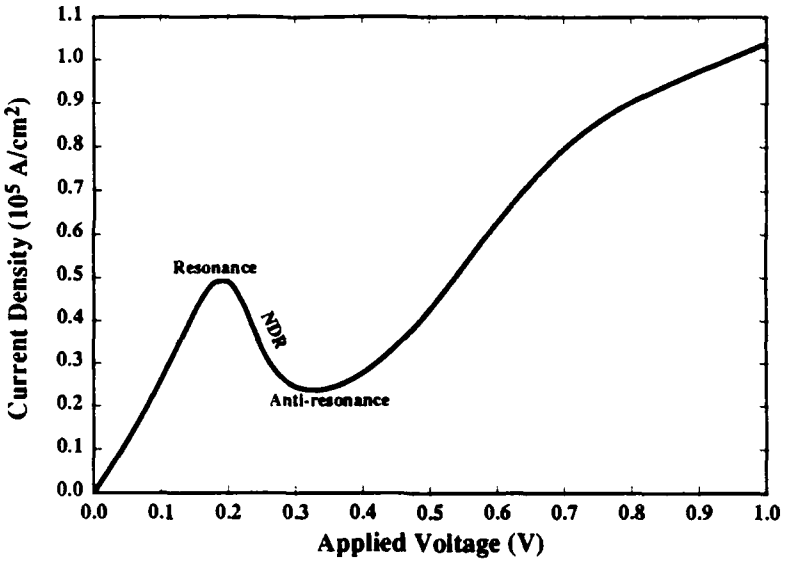

Figure 2 Simulated SiGe RTD I-V Characteristic

During the previous reporting period, a rudimentary steady-state simulation program was written, which was accurate enough to predict the characteristic negative differential resistance (NDR) region of operation of an RTD. The simulated I-V characteristic of the SiGe RTD in Fig. 1 is shown in Fig. 2. The shape of the I-V curve, including a peak corresponding to resonance of the RTD and a valley corresponding to anti-resonance, indicated that the simulator was giving reasonable results. The voltage bias at resonance was also reasonable for the RTD in Fig. 1. GaAs RTD structures were also simulated, with similarly reasonable results.

During the past year, several improvements have been made in the quantum device simulator. One of these was the addition of the capability to calculate (from the WF) and plot the carrier density versus position in the RTD. Figure 3 shows the hole density for the SiGe RTD in Fig. 1 at zero applied bias. (The hole density decrease at the device/contact interface is due to numerical approximations which are discussed in more detail later.) Calculation of the carrier profile was added in anticipation of implementing self-consistency, which requires that the energy band profile and the charge density be consistent with each other. At present, we use an approximate energy band profile for the RTD (see Figure 1) in calculating the WF. We do not at present make sure that the calculated carrier density is consistent with the assumed energy band profile. Also in anticipation of implementing self-consistency, the simulation program was generalized to accept an arbitrary piecewise-constant 1-D energy band structure, rather than being limited to the structure of the RTD. Although all of our simulations to date have been done on the RTD, this modification allows us to simulate the current flow through an arbitrary quantum-scale heterostructure. We are still studying how best to implement self-consistency (see the next section).

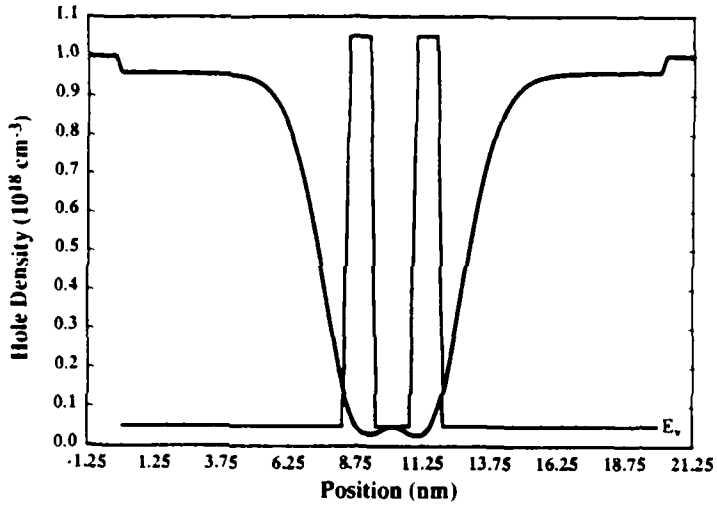

Figure 3 RTD Equilibrium Hole Density Profile

Another important improvement of our quantum simulation tool during the past year was the development of a graphical post-processor, which adds the ability to create publishable quality surface plots. A surface plotting capability was especially needed in order to view the Wigner function itself, which is a quantum probability function showing the carrier distribution in the device. Being able to view the Wigner function allows us to see in detail what is occurring in the device, an absolute necessity for meaningful research of a device. For the SiGe RTD in Fig. 1 at 0.2 V applied bias (resonance), the Wigner function is as shown in Fig. 4. This plot shows several quantum effects occurring, including quantum interference, tunneling (note the small "beam" of tunneling holes exiting the device at the cathode), exclusion from the well, and a negative quantum probability of finding carriers (holes) in some regions of phase space.

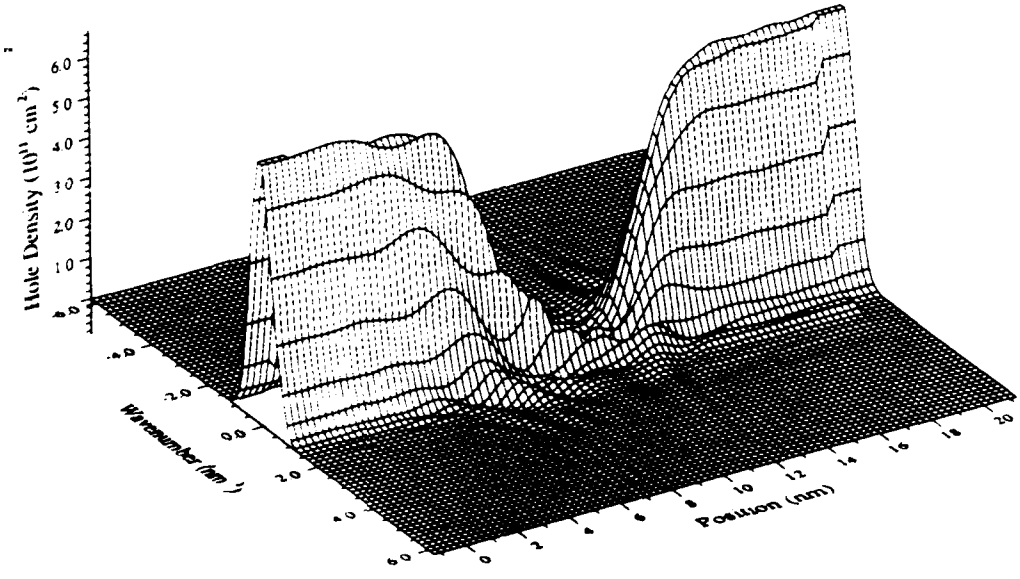

Figure 4 RTD Resonance Wigner Function

During this reporting period, we also developed a transient simulation capability. With our transient quantum device simulator, the state of the RTD is established at one (steady-state) applied bias, the bias is switched instantaneously at time zero, and we then allow the system to evolve freely towards the new steady state. We performed a transient simulation by switching the applied bias from 0.2 V (resonance) to 0.3 V (anti-resonance). Figure 5 shows the resulting current at the cathode terminal of the SiGe RTD. Note that switching occurs in 70-80 fs, which is indeed fast, but not unreasonable, considering analytical predictions [Weil] and experimental measurements [Sollner]. The most significant feature in Fig. 5 is the large pulse of current that exits the device at the cathode, peaking at about 25 fs. The cause of this can be seen from the plot in Figure 6 of current versus position in the RTD as well as time. Here we see that this pulse started in the quantum well (center layer) just after the bias was switched. This indicates that the pulse is due to charge emptying out of the well. We also see a similar pulse exiting the device at the anode, which is due to holes reflecting off the anode barrier and propagating back to the anode contact.

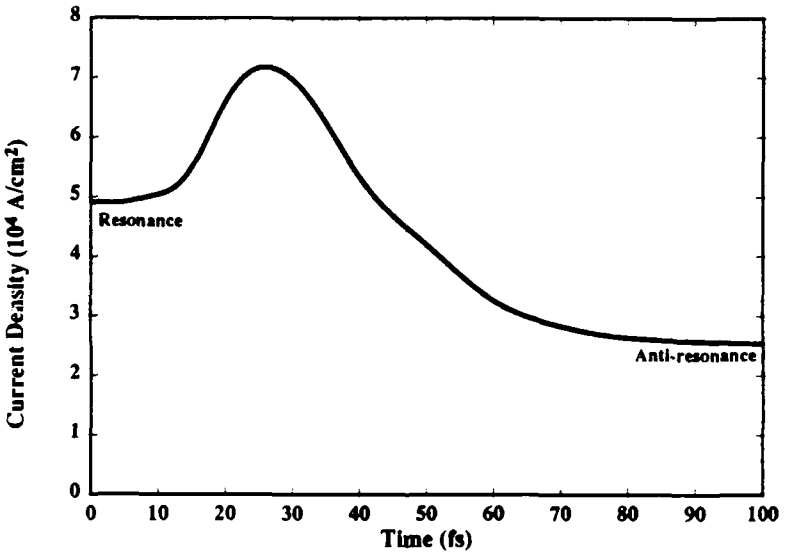

Figure 5 RTD Transient Cathode Current

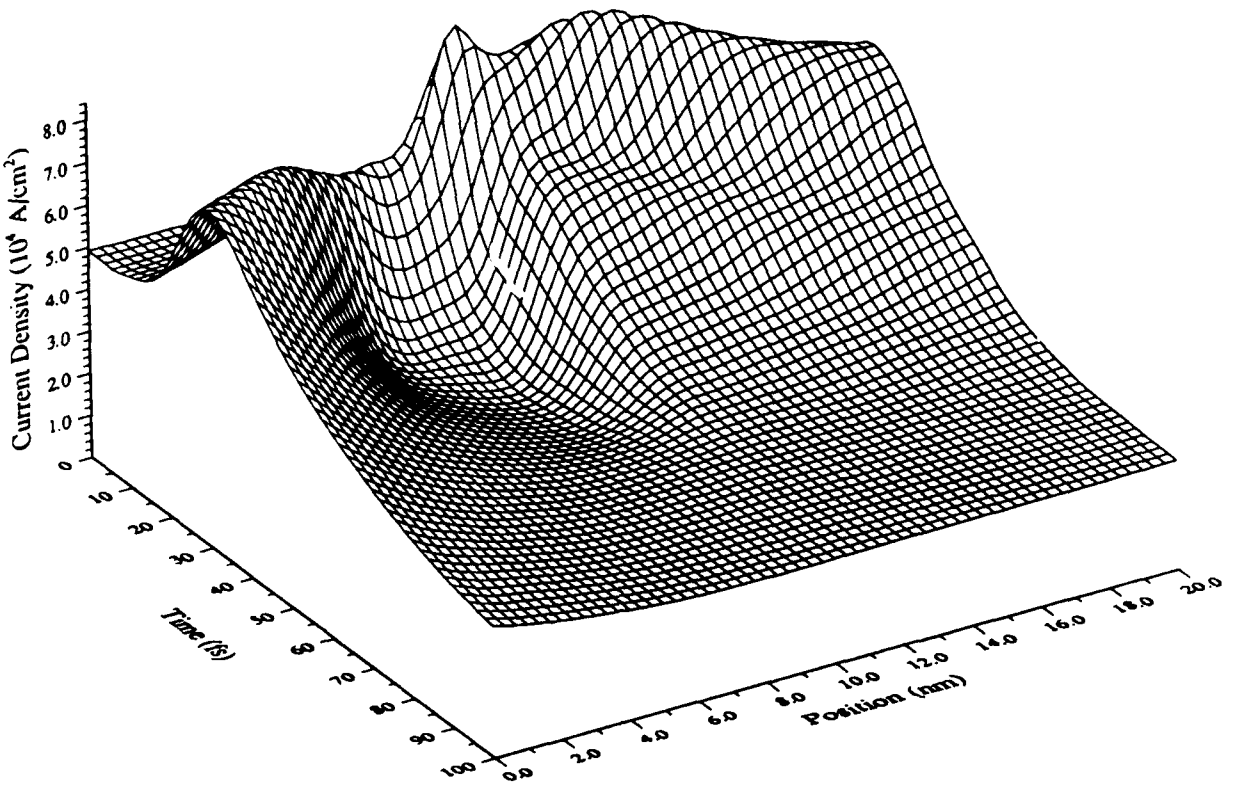

Figure 6 RTD Transient Internal Current

A great deal of effort has been applied during the past year to improving the accuracy of our numerical implementation of the WF QTE. In order of significance to the accuracy of the simulation, some issues that we have investigated are: 1) using a higher order finite difference approximation for derivatives (Figs. 1-6 used a first-order approximation), 2) varying the fineness of the position and wavenumber (velocity) grid, 3) varying the width of the contact regions, and 4) having a position-dependent versus constant effective mass along the RTD. To illustrate some of these complexities, consider the Wigner function shown in Fig. 7, which was calculated exactly as that in Figure 4, but using a second-order finite difference approximation. Note especially the much larger tunneling current "beam" (about a factor of 5 larger) and the much greater amount of structure in the Wigner

function. We believe that the larger tunneling current is real, since this feature remained roughly constant for finer grid simulations. In fact we might expect this result that such non-linear phenomena as tunneling are more accurately modeled by higher order simulations. There is also a lot more structure in the calculated Wigner function calculated using this second-order approximation method. This is not surprising, since we know [Barker] that a great deal of structure appears in wavefunctions that are incident on abrupt barriers. We found that the structure on the anode (lower x) side of the RTD remained in finer grid simulations, while much of that on the cathode side smoothed out. Clearly, the task of making accurate simulations and interpreting simulation results are not straightforward (for more details, see [Jensen 2]. We are still working to improve our numerical implementation of the WF QTE to accurately model these quantum systems, which requires not only that we correctly simulate real phenomena, but also that we do not, through an inadequate numerical implementation, create imaginary phenomena.

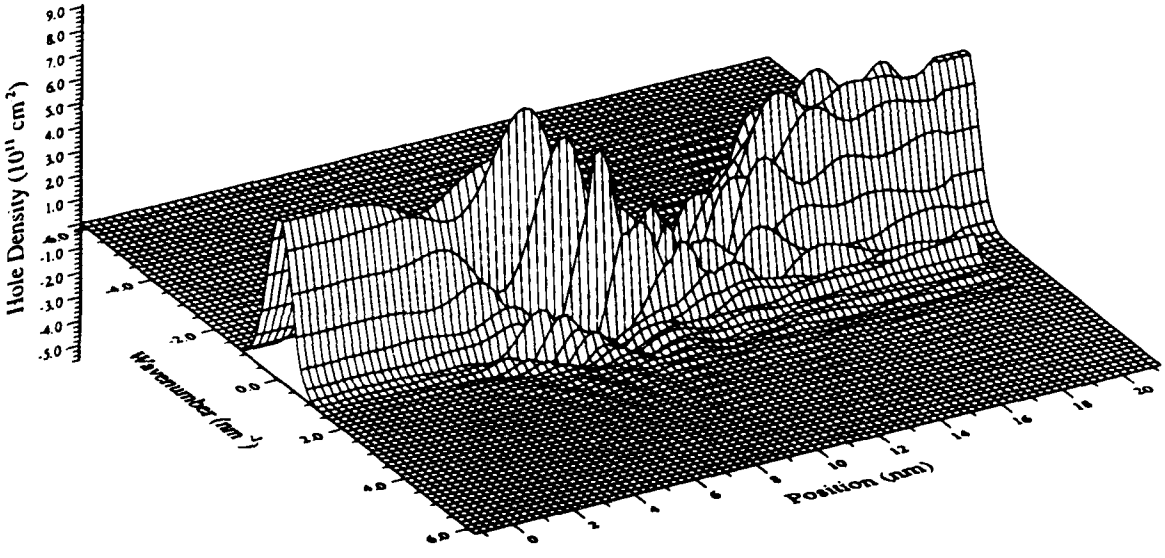

Figure 7 Second-order RTD Resonance Wigner Function

Our final objective is to experimentally investigate particular quantum-scale structures in the SiGe material system. Because this phase of our work will begin during the next reporting period, more will be said about this objective in the next section. However, based on our simulation results, we can make some initial remarks about the suitability of using the SiGe material system, especially in comparison with the GaAs system, for quantum-scale devices. Heterostructures in the SiGe system exhibit most of their energy band offset in the valence band, so that quantum devices (which are based on quantum-scale energy band offsets) must be p-type. On the other hand, quantum devices in the GaAs system are n-type. Further, because of the higher effective mass of holes in SiGe versus electrons in GaAs, the wavelength of carriers in SiGe is shorter and therefore layer thicknesses must be smaller to take advantage of quantum effects. The SiGe RTD used in this report is and extreme example (only two monolayers in the barriers and three in the well). However, the very thin barriers and quantum well were only used to give relatively wide resonances, making accurate simulation easier. In practice, one can use thicker barriers while accepting lower current densities, and a wider well if one can accept lower bias voltages and higher valley currents. These simulations have demonstrated that, in principle, it is possible to produce the same quantum effects in SiGe structures as in GaAs structures, although with smaller structures. We have also noticed that quantum effects are more sensitive not only to the numerical parameters of the simulation, but also to the exact device structure in SiGe than in GaAs devices. This indicates that structural control will be more critical in SiGe quantum devices. None of these conclusions negates the usefulness of experimental investigations of quantum devices in the SiGe material system.

3. Goals

In the future, this work will continue to evolve from theory to simulation to experiment. We will continue our theoretical investigation of quantum computing, since insight and analysis in this area will indicate whether and how quantum computing will become reality. Work on our quantum device simulation programs will continue as well. Several important improvements are planned:

1) Self-consistency. This requires that the carrier distribution as calculated from the Wigner function is consistent with the energy band profile that was used to calculate the Wigner function. Implementing self-consistency will require an iterative solution of the Wigner function QTE. We believe that we should be able to guess (for the RTD) the energy band profile fairly closely, so that only on the order of 10 iterations may be required. Self-consistency is needed to reasonably compare simulation results with measurements of real devices.

2) Dissipative effects. Either a relaxation time approximation or a more accurate method may be used.

3) Numerical robustness. We will continue to work for a more user transparent quantum device simulator, which can give accurate simulation results given any reasonable energy band structure.

4) More physical boundary conditions. We will investigate the effect of different boundary conditions (e.g., drifted versus equilibrium Maxwell distribution) on the solution of the QTE.

5) Equivalent circuit generation. Although we see from Figs. 4 and 7 that the internal operation of quantum devices like the RTD is very complex, we will investigate the possibility of using simulation results, especially terminal characteristics of the device, to generate lumped parameter "equivalent" circuit models. If reasonably accurate models can be found, this approach would allow us to easily incorporate these devices into circuit simulators and to thus see how independent quantum devices would function in a larger circuit.

In parallel with our simulation effort, we will begin the experimental phase of our work, in which we plan to fabricate the quantum-scale structures that we are simulating to test the simulator's predictions. Of course, the goal is always to use simulation to guide experiment as well, so that each area of research benefits from the other. Of the above planned improvements to our quantum device simulator, at least self-consistency must be implemented before its results can be reasonably compared with experimental measurements. However, we have decided to begin fabricating structures for measurement immediately, because we expect it to take some time to get a working process in place for the fabrication of functional SiGe RTD structures. Two experienced research teams have offered to produce the material, including the basic RTD layers, for these devices. We will fabricate the actual device structures ourselves. We have chosen to use the SiGe material system in these experimental investigations because sufficient n-type quantum device data has already been produced by other researchers. Being able to compare our results with p-type device results will help to assure that our simulation tool is as general as possible.

We are strongly committed to the publication of any and all conclusions we arrive at, whether positive or negative, concerning quantum computing in general, the Wigner function simulation approach, and the use of SiGe as a material basis for quantum-scale devices and systems. Thus, although no publications have resulted from this work as yet, work is proceeding on one or more potentially publishable papers. In particular, work is

proceeding on a intermediate level general review of quantum computing in terms of theory and numerical simulation. Such a review is greatly needed in this field, as it can increase the general level of awareness, understanding, and interest.

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Unit: 8

TITLE: Applications of SiGe in MOS Technologies

PRINCIPAL INVESTIGATOR: K. C. Saraswat

GRADUATE STUDENT: T.-J. King

Scientific Objectives

The objective of this work is to investigate various applications of the semiconductor alloy silicon-germanium (SiGe) to MOS technology. Because the physical and electrical properties of SiGe can be tailored by changing its Ge content, the use of SiGe can allow more flexibility in the design of a MOSFET process. In the current reporting period, we have investigated the use of polycrystalline SiGe as the gate material in an MOS technology.

Introduction

As the dimensions of CMOS devices are reduced, the high resistivity and low workfunction of N+ poly-Si, the material traditionally used for the gate electrode, are becoming increasingly problematic. The high resistivity results in large *RC* delays, while the low workfunction requires the use of buried-channel PMOS devices which are not as easy to scale down in size compared to surface-channel PMOS devices due to punch-through and drain-induced barrier-lowering effects [Hu]. Several techniques have been suggested to overcome these problems for submicron CMOS technologies, *e.g.*the use of dual N+/P+ doped polycide gates [Hillenius], and the use of a direct tungsten gate [Wong]. Although these alternatives provide surface-channel NMOS and PMOS devices, they have practical limitations (*i.e.*lateral dopant diffusion in the connected N+ and P+ polycide gates causing threshold-voltage instabilities [Hillenius], and incompatibility of tungsten with Si fabrication processes) which make them difficult to implement in manufacturing. In the work which has been completed during the reporting period, we have shown that P+ doped polycrystalline SiGe is an attractive alternative for the gate material in a CMOS technology, because it allows both NMOS and PMOS surface-channel devices to be achieved.

Physical Characterization of Polycrystalline SiGe

The poly-SiGe films used throughout our work were deposited in a conventional hot-wall low-pressure chemical vapor deposition (LPCVD) system, using silane (SiH_4) and germane (GeH_4) as the gaseous deposition sources, at pressures between 100 mT and 200

mT. The SiH_4 flow rate was kept constant at 25 sccm; the films were deposited at various temperatures: 500°C, 550°C, and 625°C. The thicknesses of the deposited films were determined by using a masked etch and measuring the step height using a surface profiler. From these measurements of film thicknesses, the deposition rate was found to increase significantly with increasing GeH_4 flow rate. With the trend toward single-wafer processing, the enhanced film deposition rate is useful, since it would improve wafer throughput.

A standard poly-Si plasma etch process was used to pattern the films. The etch rates for the poly-SiGe films were found to be higher than for a poly-Si film, so that the selectivity of the etch process is better for poly-SiGe films than for poly-Si films. The Ge mole fractions of the deposited films were determined by Rutherford Backscattering Spectrometry (RBS). As shown in Fig. 1, the percentage of Ge in the deposited films increases linearly with the percentage of GeH_4 in the deposition source gas. The practical deposition and etch rates, combined with the linear variation of Ge mole fraction with GeH_4 flow rate, make the formation and patterning of poly-SiGe films very controllable processes.

X-ray diffraction (XRD) analyses were performed on the deposited films to study their crystal structure. Each step scan contained several singular peaks characteristic of a polycrystalline material with the diamond cubic crystal structure. The peak locations were located in-between those of pure Si and pure Ge, and were shifted more towards those of pure Ge for the films with higher Ge content (Fig. 2). The films were also examined using Transmission Electron Microscopy (TEM). Diffraction patterns taken from single poly-SiGe grains showed only one set of rings characteristic of a diamond crystal structure. Thus, the XRD and TEM analyses confirm that the deposited films are SiGe alloys, rather than clusters of Ge within a Si matrix. The TEM transmission patterns showed that the grain structure of the poly-SiGe films was essentially the same as that of the poly-Si films; however, the average grain size in the as-deposited films was larger for the films with higher Ge content.

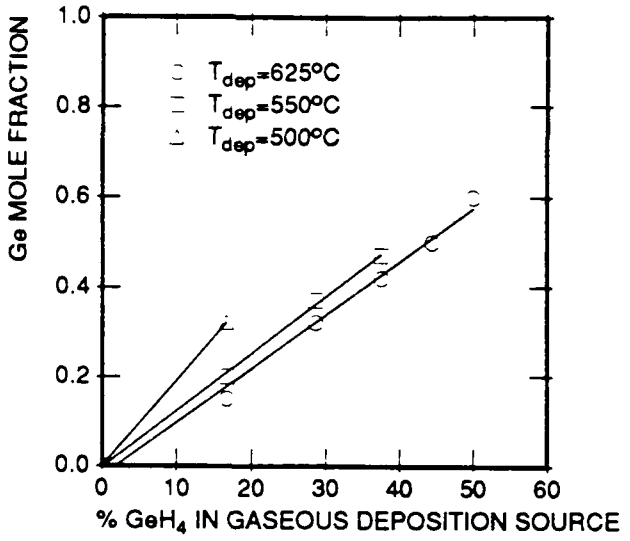

Figure 1: Ge mole fraction (as determined by Rutherford Backscattering Spectrometry analysis) *vs.* GeH_4 flow.

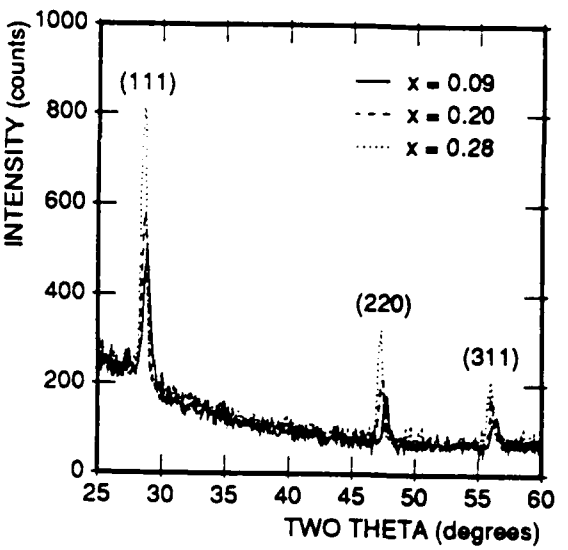

Figure 2: X-ray diffraction step scans of poly-$Si_{1-x}Ge_x$ films.

Electrical Characterization of Polycrystalline SiGe

Rapid thermal annealing (RTA) was used to study the dependences of film resistivity on anneal temperature and boron implant dose. Approximately 3000 A-thick films were implanted with boron, at an energy of 20 keV, and then annealed for 30 seconds at successively higher temperatures. In Fig. 3, the resistivity is plotted as a function of anneal temperature, for a boron implant dose of 1 x 10^{15} cm^{-2}, for films of various Ge content. It is evident that the anneal temperature required to activate the boron decreases dramatically as the Ge content in the film increases. Alternatively, approximately half as much boron is needed for the poly-SiGe films in order to achieve a resistivity comparable to that of poly-Si. Hall measurements indicate that the reduction in resistivity with increasing Ge content is the result of a significant increase in dopant activation along with a slight increase in hole mobility. This reduction in required dose and anneal temperature may help assuage the problem of boron diffusion through the thin gate oxide in a submicron P+ gate CMOS technology [Pfiester].

MOS capacitors of various gate-oxide thicknesses were fabricated on 5-10 W-cm N- and P-type substrates using N+ and P+ poly-SiGe films as the gate material. The gate-to-semiconductor workfunction difference, F_{MS}, was extrapolated from the plots of flatband voltage vs. oxide thickness, for both N+ and P+ poly-SiGe films of various Ge mole fractions. The measured decreases in gate workfunction with Ge content for the PMOS capacitors were in good agreement with those measured for the NMOS capacitors. The extrapolated F_{MS} values for the PMOS capacitors are plotted as a function of Ge mole fraction in Fig. 4. A slight decrease in F_{MS} was observed for the N+ poly-SiGe gate capacitors. The data shows that the workfunction of poly-Si decreases with Ge content, and that the reduction in the Si bandgap is due predominantly to the change in valence band energy, as is the case for a single-crystal SiGe material [King].

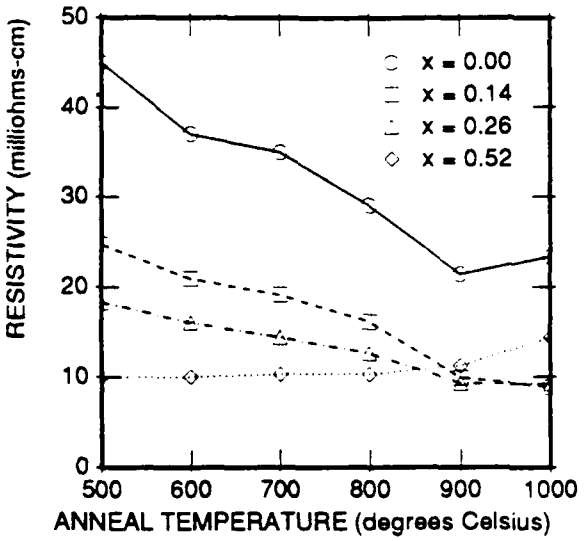

Figure 3: Resistivity of poly-$Si_{1-x}Ge_x$ films implanted with 1 x 10^{15} cm^{-2} Boron, then annealed (RTA) for 30 seconds at successively higher temperatures.

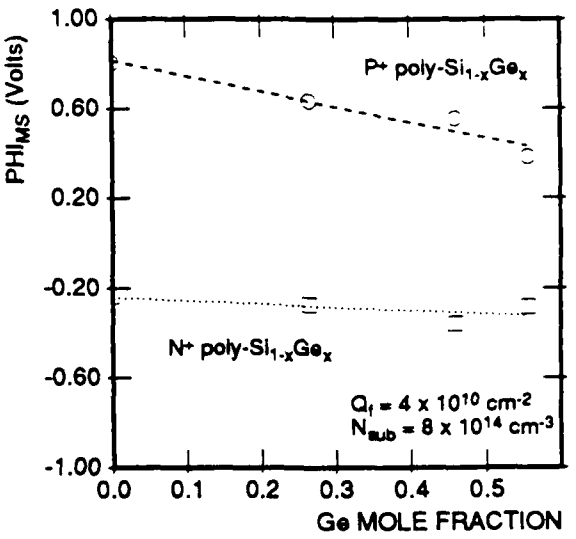

Figure 4: Gate-to-semiconductor workfunction difference for poly-$Si_{1-x}Ge_x$ gate PMOS capacitors, extrapolated from measurements of V_{FB} *vs.* oxide thickness.

Transistor Characteristics of SiGe-Gated MOSFETs

Simple NMOS and PMOS transistors were successfully fabricated to demonstrate the practicality of using poly-SiGe as the gate material, using Stanford's standard 2 mm CMOS process. The shift in threshold voltage due to the presence of Ge in the gate material was apparent from the PMOS and NMOS transistor *I-V* characteristics.

The short-channel behavior of NMOS and PMOS transistors was examined by use of numerical process [Hansen] and device [Pinto] simulation. Typical parameters for a submicron CMOS process were chosen, and the threshold-adjust implant doses were selected to give nominal threshold voltages of 0.7 V for long-channel (5 mm) devices. The results of the simulations showed that NMOS transistor short-channel behavior is noticeably better for a P+ poly-SiGe gated device than for a P+ poly-Si gated device, and that the short-channel behavior of the PMOS device is not compromised by using P+ poly-SiGe as the gate material rather than P+ poly-Si. In fact, because the P+ poly-SiGe gate device requires a lower channel surface doping concentration, the surface mobility and subthreshold slope are improved slightly over that of the P+ poly-Si gate device.

Discussion

The results of the physical characterization work show that Ge can be easily incorporated into poly-Si to form a SiGe alloy. The thickness and compositional uniformities for deposited poly-SiGe films were as good as those of deposited poly-Si films. Poly-SiGe films of up to 60% Ge content were not affected by the chemical solutions typically used in silicon processing. Also, the morphology of the films was not changed by high-temperature (up to 950°C) annealing in argon or in oxygen. The electrical properties (*i.e.*resistivity, workfunction) of the poly-SiGe films were found to be very uniform across a wafer. Therefore, poly-SiGe films are completely compatible with standard VLSI fabrication processes; their use as gate material does not introduce additional process complexity into a poly-Si gate CMOS technology.

A P+ poly-SiGe gate CMOS technology is advantageous compared to either a P+ poly-Si gate or an N+ poly-Si gate CMOS technology. In contrast to a P+ poly-Si gate technology, a P+ poly-SiGe gate technology has NMOS devices with improved short-channel behavior, due to the reduction in the counterdoping implant dose required to achieve the nominal threshold voltage (0.7 V). It also results in PMOS devices with acceptable short-channel behavior. Since buried-channel NMOS devices can be made more punch-through resistant at short channel lengths than buried-channel PMOS devices [Parrillo], a P+ gate CMOS technology should be more scalable than an N+ gate CMOS technology.

By increasing the Ge content of the P+ poly-SiGe gate material, the gate workfunction could conceivably be decreased to such an extent that the required counterdoping implant dose falls below the amount which would cause an *n-p* junction to be formed in the NMOS channel region (*i.e.*all of the implanted arsenic in the channel region is depleted). In this case, the peak electric field would be located at the surface (in contrast to a typical buried-channel device, in which the peak electric field, and therefore the current path, is located below the surface), so that surface-channel operation would be achieved under turnoff conditions. At the same time, the higher channel mobility due to the reduction in transverse electric field would be preserved [Parrillo]. However, as the gate workfunction is decreased, the short-channel behavior of the PMOS device may be compromised due to the decreased channel doping required to maintain a fixed threshold voltage of -0.7 V. Since the amount of reduction in the gate-material's workfunction is determined by its Ge content, the tradeoff between the PMOS and NMOS channel-doping designs can be adjusted by varying the Ge mole fraction in the gate material. It should be noted that for a CMOS technology which has relatively low channel background doping concentrations (*e.g.*less than 5×10^{16} cm^{-3}), such as a CMOS silicon-on-insulator (SOI) technology, the use of a single P+ poly-SiGe gate material can result in both surface channel PMOS and

NMOS devices, since the NMOS native threshold voltage is low enough so that the lower gate workfunction will require a non-compensating threshold- adjust implant to achieve the nominal threshold voltage.

Future Work

During the next year our objective is to develop GeSi on insulator (GSOI) thin film transistor (TFT) technology and apply it to state-of-the-art static RAMs and large area display drivers. Presently, TFTs are fabricated in polycrystalline Si films. Most of the electrical and physical properties of the TFTs are controlled by grain boundaries. Dopant segregation, carrier trapping, anamolous thermal oxidation, and enhanced dopant diffusion are some of the effects of the grain boundaries which severely limit the opportunity to exploit this technology. In order to minimize the impact of grain boundaries, the major requirements are larger grain size in the film and process steps which require relatively low temperatures and short times. These requirements are not easily met in a polycrystalline Si thin film technology. We believe that a polycrystalline GeSi thin film technology will open up a large number of exciting opportunities in this context.

Poly-GeSi films can be deposited by LPCVD in commercially available equipment and have the potential of providing larger grains and lower thermal budget processing. In addition, P+ GeSi films used as the MOS gate electrode offer variable gate workfunction and hence can be used to optimize the performance of the MOS transistors. Specifically, we will 1. Complete the development of the technology for low pressure chemical vapor deposition (LPCVD) of GeSi thin films in a hot wall tubular reactor; 2. characterize the physical and electrical properties of GeSi thin films; 3. assess the compatibility of GeSi thin films with state-of-the-art VLSI processes; and 4. fabricate and characterize PMOS and NMOS transistors in GeSi thin films using GeSi gates, with possible applications to SRAMs and large area display drivers.

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Unit: 9

TITLE: Packet Equalization

PRINCIPAL INVESTIGATOR: J. M. Cioffi

GRADUATE STUDENTS: H. Bims, K. Wilson and R. Ziegler

MATRICULATED PH.D. STUDENTS: J. Aslanis

Scientific Objectives:

The scientific objective has been the study of signal processing and coding methods that enhance the performance of digital mobile communication links. Focus has been on reliable transmission in the presence of time-varying multipath and adjacent-channel distortion.

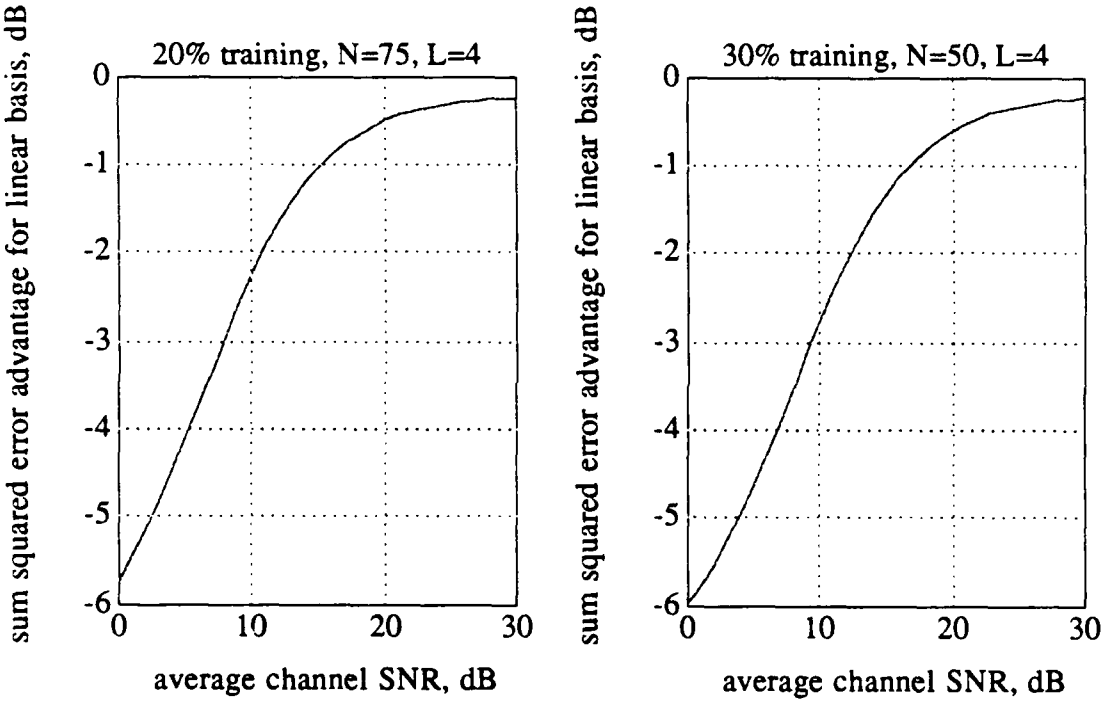
Summary of Research:

Emerging digital portable data transmission formats, such as time-division multiple access (TDMA) methods (for example, the North American TIA/IS-54 or the Pan-European GSM standard) and code-division multiple access (CDMA) methods, are based on packetization of the transmitted data stream into relatively short blocks (few hundred bits or less) or packets. We have examined several signal processing and detection issues arising in such packet digital communication schemes. We call the reliable reception of such packets generally packet equalization. In particular, we describe some work related to the issue of receiver training in the next section and then progress to the subject of equalization methods to mitigate crosstalk.

Packet Equalization

A standard procedure in packet detection is to transmit some known sequence of data symbols (the training sequence) as part of the data block, which can then be used by the receiver to estimate the channel response. The estimated channel response is used to detect the unknown (information) symbols that comprise the rest of the block. A usual assumption is that the channel is constant over the duration of the block, even in fading-channel communication. We have investigated the validity of that assumption, both in understanding the degradation in receiver performance caused by actual intra-block channel variation, and in studying the performance of channel estimates using channel models with explicit time variation. The former goal was readily accomplished, in that we could compute the degradation in the quality of the channel estimate; however, directly tying this

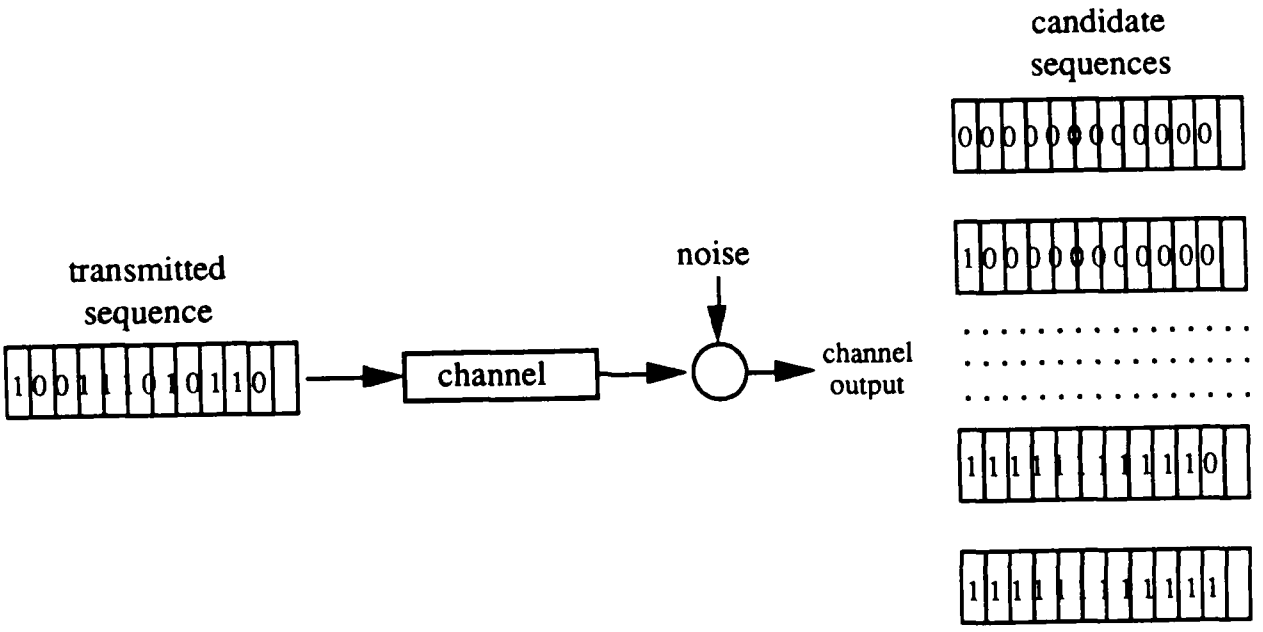
to a more interesting measure of quality, like probability of symbol detection error, proved to be a more difficult task. As to the use of time-varying channel models, we found little or no performance improvement over the standard constant channel assumption for typical mobile radio communication scenarios. The following plots compare the performance when using a constant channel assumption versus a model with both a constant and a linear (in time) basis for the channel parameters. The actual channel has flat power-delay profile and is fast-fading. The data block sizes are indicated by the parameter N, and the length of the channel memory in symbol periods is L=4. We see that for average signal-to-noise ratios up to 30 dB, the constant channel assumption results in estimates which are superior to those produced by the time-varying model.



Our results suggest that while the constant-channel assumption is rarely true (and channel estimate quality can be significantly affected by the time variation), in practice one can't do much better than the constant channel assumption within a reasonable sized packet. What was apparent from our study was that the percentage of training and how the training sequence is placed and used within the packet is more important that fitting a time-varying model to the packets. That is, even for long packets with significant time variation over the packet, one uses a constant channel approximation within subpackets, each of which must contain a certain amount of training or pilot data that is used to update the channel model. We are now further pursuing this observation and its implications.

Along this pursuit, it is desirable from a probability of error perspective to have as accurate a channel model as possible (albeit fixed between training intervals). One method to obtain a more accurate channel model is to use a greater number of training symbols; this, unfortunately, reduces throughput. One major focus of our research is the determination of the smallest training-to-overall data ratio required to send reliable data at the highest data rate. While we have many ideas that appear promising, we will only report further here on what we presently know.

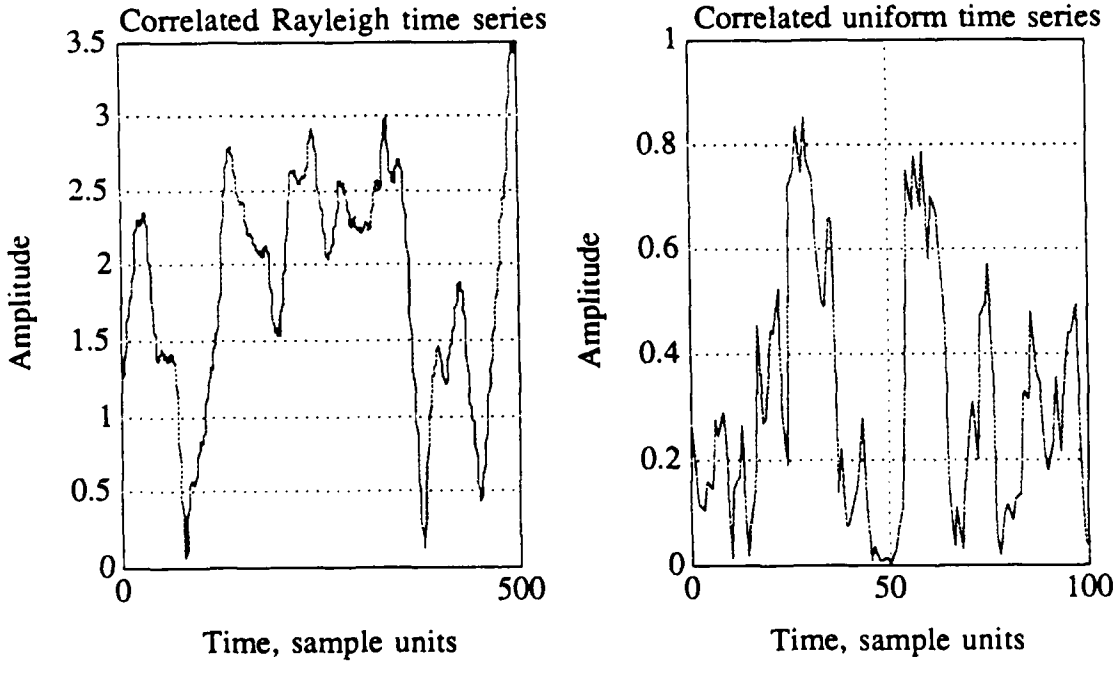
We considered *joint* estimation of both the channel parameters and the transmitted data sequence. In its simplest form this consists of computing a maximum-likelihood (ML) estimate of the channel response, for each possible transmitted data sequence. The likelihood function is, in the case of additive Gaussian noise, proportional to the squared norm difference between the received signal sequence and the reconstruction of that sequence given the transmitted data sequence and the ML channel estimate. The *joint* ML estimate is that which maximizes the likelihood function over all the possible transmitted data sequences.



Results of this study were very surprising in that we found that it was possible to use extremely short training sequences to attain very high performance levels. For instance, on a channels with memory that spanned 10 symbol periods, conventional equalization methods require hundreds of symbols to train, while emerging fast equalization methods used in GSM and IS-54 require 20-30 symbol periods to synchronize and train the receiver. In our study of joint maximum likelihood, we were able to get better performance than these methods using only 4 to 5 training symbols. The reader should be alerted that the complexity required to implement a real receiver (we used off-line computer simulation to obtain our results) is enormous. Nevertheless, we are now pursuing alternatives that we hope will achieve similar performance with reduced complexity.

Generation of Rayleigh Processes

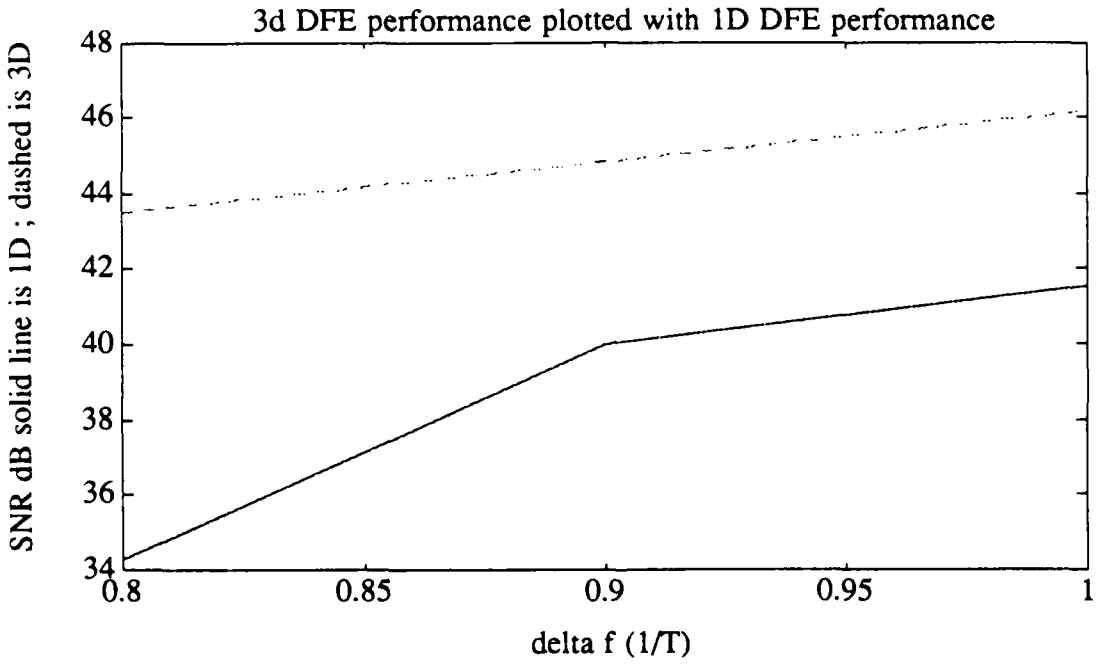
As an aside, we developed a general technique for producing correlated random variables or samples of random processes with arbitrary marginal distributions. This was a necessary tool in simulation studies of time-varying channels. Although certain technical issues remain unexplored, the method could be useful for other applications also. The following plot shows two examples of processes that can be obtained with this technique.



Diversity

This Rayleigh generator has been used to simulate flat fading in time varying mobile channels, a situation where antenna diversity can be very attractive. However, to effectively use diversity, one needs to use some amount of training. We have found that our earlier results on the issue of the amount of training versus the performance improvement can also be used to improve the operation of a packet equalization system that simultaneously processes the outputs of all the antennae.

Multidimensional Reception



Multidimensional Reception

A multidimensional decision feedback equalization (DFE) method has been investigated for the mitigation of the adjacent channel interference that can often appear in mobile data transmission. The method essentially samples at a sufficiently high rate to capture adjacent channel signals and a multidimensional equalizer is used to mitigate crosstalk interference along with intersymbol interference. When adjacent channel spacing is close and crosstalk is the dominant noise source, large gains in effective signal-to-noise ratio are exhibited by multidimensional equalization as seen in the above figure. The trade-off for the improvement is an approximate doubling to tripling of receiver computational requirement. The method allows center frequencies to be placed closer together, with a guard band every third frequency. This method is described in [Wilson 90].

References (JSEP Supported)

Most of the references that are listed here are the result of work that was previously supported by JSEP. Only the Wilson, Ziegler and Bims references are pertinent to the present research described in this report.

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Unit: 10

TITLE: Fast Arithmetic Computing with Neural Networks

PRINCIPAL INVESTIGATOR: T. Kailath

GRADUATE STUDENTS: G. Xu, K.-Y. Siu

Scientific Objectives:

In the past year, studies in the area of artificial neural networks have been focused in the following areas:

- A New Class of Fast Arithmetic Circuits based on the Neural Network model
- Depth-Size Tradeoffs in Neural Computation
- A New Geometric Approach to the Analysis of Neural Networks

Summary of Research:

A. A New Class of Fast Arithmetic Circuits

Before we summarize our results in this area, we shall first give some background and motivation for our work.

The basic processing element of a neural network is a *neuron*. The common model of a neuron is a device that computes a *linear threshold function* f :

$$f(X) = sgn(F(X)) = \begin{cases} 1 & \text{if } F(X) \geq 0 \\ -1 & \text{if } F(X) < 0 \end{cases}$$

where

$$F(X) = \sum_{i=1}^{n} w_i \cdot x_i + w_0.$$

Here X is an n-dimensional vector with components that can be real valued or just binary. The real valued coefficients w_i are commonly referred to as the *weights* of the threshold function.

It is well known that linear threshold elements can simulate digital logic gates such as AND, OR, NOT. Therefore, we can perform digital arithmetic such as addition and multiplication using neural networks. The basic problem is that multiplication cannot be done in a digital circuit with bounded delay. One of the basic assumptions in the study of

neural networks is that we allow the neural elements to take on an unbounded number of inputs, i.e. we allow *unbounded fan-in.* Perhaps this feature of neural elements can give rise to a significant increase in computing power? In fact, by exploiting this feature, we are able to show the following interesting results: *the sum and product of two n-bit numbers, and sorting of n n-bit numbers can all be done with 4 unit delays with neural networks.*

Recently, using classical results from number theory and our previous results in computing multiplication, we have extended our results to more complicated functions and have shown that exponentiation and division can be computed with 5 unit delays, and multiple product can be computed with 6 unit delays, with neural networks.

Of course, the practical issues of building such (large fan-in) neural networks using physical analog devices still remain. If the implementation of such artificial neural elements is made possible by advances in future technology, it would mean that we can have an ultra-fast parallel computer built of such elements.

In the meantime, we have explored some other practical aspects. For example, since we would like to implement a neuron using analog devices, from a practical point of view, it is important to see if the assumption of real valued weights is necessary. In fact, we have been able to show that our results hold for a restricted class of neurons in which only $O(\log n)$ bits accuracy is required for each of the weights.

B. Depth-Size Tradeoffs in Neural Computation

Another important issue that we have pursued recently is the trade-off between the *size* (*i.e.* number of threshold elements) and the *depth* (*i.e.* number of unit delays) of neural networks. This issue arises naturally in the implementation of neural networks. Sometimes when the time for the computation is not as crucial, we might want to have a smaller network at the expense of a slight increase in the time for computation. In other words, we want to investigate if increasing the depth by a small constant factor can greatly reduce the number of linear threshold elements in the network. In fact, our most recent work has given a positive answer to this question. The best known results (Minnick '61) in computing any symmetric boolean function of n variables with neural networks require $O(n)$ threshold elements and two layers. It has been an open problem for 30 years to determine if the size can be be further reduced for arbitrary symmetric function. We are able to show that by increasing the depth by one, i.e. by using a 3-layer neural network, we can reduce the number of elements to

$O(\sqrt{n})$. For functions with a 'periodic structure' such as the parity, we have extended the depth-size tradeoffs results to higher depth: for every d, we can construct neural networks of depth-$(d+1)$ and size $O(dn^{1/d})$ computing them.

One would like to know if the above tradeoff results are best possible. In other words, can we reduce the size further without increasing the depth of the network? In fact, using classical results from theory of rational approximations, we have shown that our construction of the network is almost optimal in size; any depth-3 neural network computing an arbitrary symmetric function will have size at least $\Omega(n^{1/2-\epsilon})$ for any $\epsilon > 0$. For functions with a 'periodic structure' such as the parity, the lower bound results can be extended to higher depth: any depth-$(d+1)$ neural network computing the parity function will have size at least $\Omega(n^{1/d-\epsilon})$ for any $\epsilon > 0$.

C. A Geometric Approach to Neural Networks

We are currently developing a new geometric approach for investigating the power of neural networks. Our approach views a boolean function of n variables as a vector in an 2^n-dimensional Euclidean space and invokes tools from linear programming and linear algebra to derive new results on the realizability of boolean functions using threshold gates. We have obtained some preliminary results via this geometic approach. Some of the consequences and implications of our new approach are as follows: 1) it leads to an effective upper-bound on the number of spurious memories in Hopfield networks programmed by the outer-product rule; 2) it yields a much improved upper-bound on the number of distinct functions implementable by a depth-d threshold circuit; 3) it generalizes several key results in the area of threshold circuit complexity, particularly those that are based on the so-called spectral or harmonic analysis approach; 4) it leads to strikingly simple proofs for many of these earlier results, and 5) it shows the limitations of the only known technique (based on computing correlations among boolean functions) for determining lower-bounds on the depth required for implementing boolean functions using threshold gates. Our approach also yields a unified framework where many of the well known results concerning the fundamental limitation of neural networks can be derived as special cases, and without introducing too many seemingly difficult concepts.

Our new geometric approach is most promising in obtaining lower bounds on the power of neural networks. Not only are lower bound results interesting theoretically but they also provide a guideline of how good the design of our networks are. We are currently investigating

the limitation of small depth neural networks using our new approach .

Publications:

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2. K.-Y. Siu, J. Bruck and T. Kailath *Computing with Almost Optimal Size Threshold Circuits*; submitted to the Journal of Computer and System Sciences, July 1990.

3. K.-Y. Siu and J. Bruck, *On the Power of Threshold Circuits with Small Weights*; to appear in SIAM Journal on Discrete Mathematics.

4. K.-Y. Siu, V. P. Roychowdhury and T. Kailath *Computing with Almost Optimal Size Threshold Circuits*; submitted to the Journal of Computer and System Sciences, July 1990.

5. V. P. Roychowdhury, K.-Y. Siu, A. Orlitsky and T. Kailath, *on the Circuit Complexity of Neural Networks* , Proc. Neural Information Processing Conference, Denver, Nov. 1990.

Presentations at Meetings and Symposia.

Special Invited Lectures.

1. Plenary Lecture, Math. Assoc. of America Annual Meeting, Louisville, KY, Jan. 19-25, 1990.
2. Plenary Lecture, Signal Processing Workshop, Bangalore, India, Jul. 23-26, 1990

Seminars.

1. Sept. 18-19, 1989, General Electric Corporation, New York
2. Nov. 14, 1989, School of Engineering, Sunrise Club, Stanford University
3. Feb. 22, 1990, Information Systems Laboratory, Stanford University
4. Mar. 26, 1990, Center for Development of Advanced Computing, Bangalore, India
5. Apr. 27, 1990, Scientific Computing and Computational Mathematics Meeting, Computer Science Department, Stanford University
6. Jun. 5, 1990, School of Engineering, Linkoping Institute of Technology, Sweden
7. Jun. 6, 1990, Department of Electrical Engineering, Linkoping Institute of Technology, Sweden
8. Jun. 20, 1990, Indian Institute of Science, Bangalore, India
9. Jun. 25, 1990, Central Research Laboratories, Hitachi, Tokyo
10. Jun. 26, 1990, Hitachi Res. Labs., Kokobunji, Japan

JSEP PUBLICATIONS - T. Kailath
July 1989 - June 1990

Journal Papers

[1] R. Roy and T. Kailath. ESPRIT — Estimation of Signal Parameters via Rotational Invariance Techniques. *IEEE Trans. on ASSP*, 37(7):984–995, July 1989.

[2] B. Ottersten and T. Kailath. Direction-of-Arrival Estimation for Wideband Signals Using the ESPRIT Algorithm. *IEEE Trans. ASSP*, 38(2):317–327, February 1990.

[3] A. Dembo and T. Kailath. Model-Free Distributed Learning. *IEEE Trans. on Neural Networks*, 1(1):58–70, March 1990.

[4] D. T. Slock, L. Chisci, H. Lev-Ari, and T. Kailath. Modular and Numerically Stable Multichannel Statistical Signal Processing. *IETE Technical Review*, 35(2):41–51, March-April 1990.

[5] R. Roy and T. Kailath. ESPRIT - Estimation of Signal Parameters via Rotational Invariance Techniques. *J. Optical Engineering*, 29(4):296–312, April 1990.

[6] R. Roy, B. G. Sumpter, D. W. Noid, and B. Wunderlich. Estimation of Dispersion Relations From Short-Duration Molecular Dynamics Simulations. *J. of Physical Chemistry*, 94(15):5720–5729, 1990.

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Proc. SPIE 33rd Annual Inter'l. Symp. on Optical and Optoelectronic Applied Science and Engineering, San Diego, CA, August 1989:[7]-[11]:

[7] B. Ottersten, M. Viberg, and T. Kailath. Asymptotic Analysis of the Total Least Squares ESPRIT Algorithm, pages 146-157.

[8] R. Roy, M. Goldburg, B. Ottersten, L. Swindlehurst, M. Viberg, and T. Kailath. ESPRIT and Uniform Linear Arrays, pages 370-380.

[9] A. L. Swindlehurst, R. Roy, and T. Kailath. Suboptimal Subspace-Fitting Methods for Multidimensional Signal Parameter Estimation, pages 197-208.

[10] D. T. Slock and T. Kailath. Multichannel Fast Transversal Filter Algorithms for Adaptive Broadband Beamforming, pages 22–33.

[11] G. Xu and Thomas Kailath. Wideband Array Signal Processing Via Spectral Smoothing, pages 184-196.

Proc. 23rd Asilomar Conference on Circuits, Signals and Computers, Asilomar, CA, October 1989:[12]-[19]:

[12] O. Farotimi, A. Dembo, and T. Kailath. Absolute Stability and Optiml Training for Dynamic Neural Networks, pages 133–137.

[13] K. Y. Siu, A. Dembo, and T. Kailath. Complexity of Finite Precision Neural Network Classifier, pages 138–141.

[14] B. Ottersten, T. Kailath, M. Viberg, and B. Wahlberg. Stochastic Maximum Likelihood Estimation in Sensor Arrays by Weighted Subspace Fitting, pages 599–603.

[15] M. Viberg, B. Ottersten, and T. Kailath. Direction-of-Arrival Estimation and Detection Using Weighted Subspace Fitting, pages 604–608.

[16] G. Xu and T. Kailath. Array Signal Processing via Exploitation of Cyclostationary–A Combination of Temporal and Spatial Processing, pages 945–949.

[17] B. Ottersten, R. Roy, and T. Kailath. Signal Waveform Estimation in Sensor Array Processing, pages 787–791.

[18] A. Swindlehurst and T. Kailath. 2-D Parameter Estimation Using Arrays With Multidimensional Invariance Structure, pages 950–954.

[19] A. Swindlehurst, B. Ottersten, and T. Kailath. An Analysis of MUSIC and Root-MUSIC in the Presence of Sensor Perturbations, pages 930–934.

[20] K. Y. Siu, A. Dembo, and T. Kailath. Complexity of Finite Precision Neural Network Classifier, pages 668–675, Denver, CO, November 1989. Neural Information Processing Conf.

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[21] B. Ottersten, M. Viberg, and T. Kailath. Analysis of Algorithms for Sensor Arrays with Invariance Structure, pages 2959–2962.

[22] A. L. Swindlehurst and T. Kailath. An Analysis of Subspace Fitting Algorithms in the Presence of Sensor Errors, pages 2647–2650.

[23] B. Ottersten and M. Viberg. Asymptotic Robustness of Sensor Array Processing Methods, pages 2635–2638.

[24] M. Goldburg and R. Roy. Application of ESPRIT To Parameter Estimation From Uniformly Sampled Data.